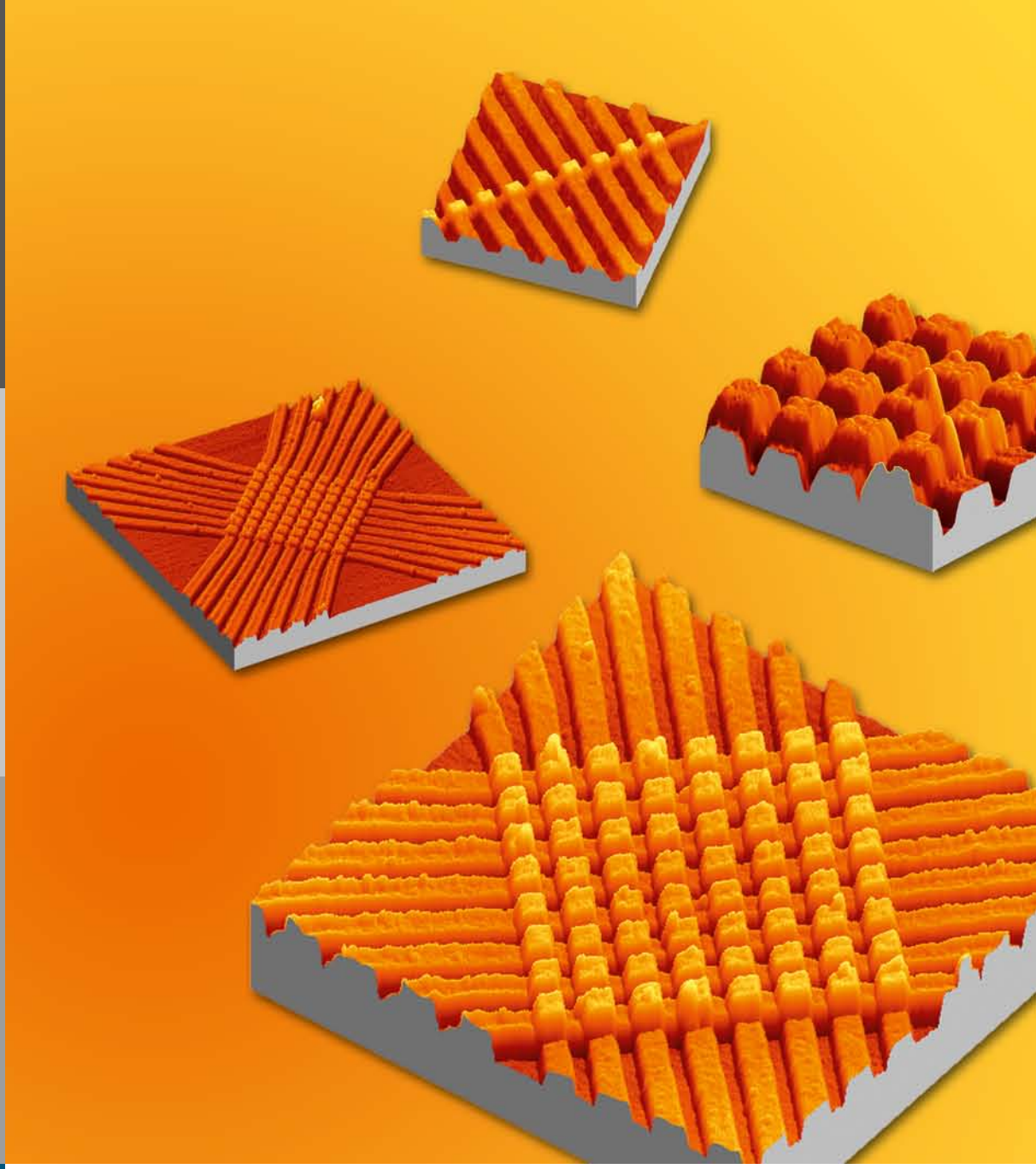

Integration of resistive switching devices in crossbar structures

Christian Nauenheim

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Kurzfassung

Die konventionelle CMOS Technologie mit optischer Lithografie als strukturbildendem Verfahren wird, genau wie die zur Datenspeicherung eingesetzten Technologien, in den nächsten Jahren an physikalische Grenzen stoßen. In dieser Arbeit werden mit der Kombination von resistiv schaltenden Strukturen als nichtflüchtige Speicherelemente oder Schalter und der Nano-Crossbar Architektur zwei Konzepte miteinander verknüpft, die die erwähnten physikalischen Grenzen nachhaltig hinaus schieben.

Bei der Nano-Crossbar Architektur wird zwischen zwei sich kreuzenden Metallleiterbahnebenen ein Funktionselement integriert. Durch die minimale Grundfläche von $4\,F^2$ (F = Minimum feature size) erlaubt diese Architektur sehr hohe Integrationsdichten. Die Grundelemente sind gerade Leiterbahnen, welche sehr gut skaliert und mittels kostengünstigen Technologien, z.B. Nanoimprintlithografie, hergestellt werden können.

Als Funktionselement wird z.B. reversibel schaltendes TiO_2 in MIM-Elementen (Metall/Insulator/Metall) integriert. Diese können durch eine entsprechende Schreib- oder Löschspannung in mindestens zwei Widerstandszustände, entsprechend logisch ‘1’ oder ‘0’, geschaltet werden. Der Zustand kann unterhalb dieser Spannungen ohne Informationsverlust ausgelesen werden.

Das Anwendungspotential umfasst sowohl Speichermatrizen, die auch als passives ReRAM (Resistive Random Access Memory) bezeichnet werden, sowie Elemente der DRL (Diode-Resistor Logic) und RTL (Resistor-Transistor Logic), Router und Multiplexer. Da es sich um passive Bauelemente handelt, kann auf eine aktive, derzeit auf CMOS basierende Infrastruktur nicht verzichtet werde. Deshalb wurde sowohl bei der Materialauswahl als auch bei der Prozessführung auf CMOS- Kompatibilität geachtet.

Durch die Entwicklung und Optimierung eines Lift-Off-Metallisierungsprozesses mit Elektronstrahllithographie wurde eine flexible technologische Plattform zur Herstellung von Leiterbahnen aus diversen Metallen bis zu einer Breite von 50 nm geschaffen. Die hergestellten Bauelemente umfassen Crossbar Arrays bis zu einer Größe von 64 × 64 bit mit Leiterbahnen aus einer 30 nm dicken Doppelschicht aus thermisch verdampften Ti und Pt. Da die Leiterbahndimensionen vergleichbar sind mit der mittleren freien Weglänge der Elektronen, wurden diese hinsichtlich ballistischer Transportmechanismen untersucht und durch das Fuchs-Sondheimer- und Mayadas-Shatzkes-Modell beschrieben. Die Leiterbahnen zeigen eine hohe Ausbeute und eine gute Skalierbarkeit mit geringen Widerständen pro Crossbar Element, selbst bei Dimensionen von wenigen zehn Nanometern.

Die TiO_2 Dünnschicht wurde reaktiv gesputtert oder per ALD (Atomic Layer Deposition) abgeschieden. Das Elektroformieren zur Überführung des Funktionselements vom isolierenden in den schaltenden Zustand wurde eingehend untersucht und erlaubte anschließend ein zuverlässiges bipolares Schalten. Die benötigten Schaltspannungen und –ströme liegen für Zellen von $100 \cdot 100\,nm^2$ bei ca. 2 V, bzw. einigen 100 µA und sind hervorragend zur

Ansteuerung in einem CMOS Hybriden geeignet. Die erreichten Widerstandsverhältnisse von mehr als zwei Größenordnungen ermöglichen eine gute Detektion der gespeicherten Information. Der einmal gespeicherte Widerstand bleibt auch bei 85°C über 10^5 s ohne Verlust stabil.

Eine Ansteuerung mit Spannungspulsen zeigte eine Schaltgeschwindigkeit <10 ns. Dabei kann der Widerstand des HRS (High Resistive State) in Abhängigkeit von der Pulsamplitude und –länge variiert werden. Die Vielzahl der auf diese Weise programmierbaren Widerständswerte eröffnet die Möglichkeit, mehrere Bit in einer einzelnen Zelle zu speichern, was die logische Speicherdichte ohne technologischen Aufwand erhöht.

Zur Untersuchung der gegenseitigen Beeinflussung der Funktionselemente eines Arrays durch das TiO_2 wurden verschiedene Bitmuster in benachbarte Zellen programmiert. Das anschließende Auslesen wies keine Interaktion von resisitiv schaltenden Zellen bis zu einem Abstand von 200 nm auf. Die Schaltcharakteristik entspricht dabei der einer Einzelzelle. In einem Array unterdrücken nichtformierte Zellen Ströme in parasitären Pfaden maßgeblich. Auf Grund der hohen Formierspannung des untersuchten Materialsystems ist die Menge der möglichen Bitmuster allerdings begrenzt.

Die Kombination der beiden Ansätze zeigte das erwartete, hohe Potential resistiv schaltender Strukturen in der Nano-Crossbar Architektur. Bei der Ansteuerung eines kompletten Arrays mit der verwendeten $Pt/TiO_2/Ti/Pt$ Kombination ist noch Optimierungsbedarf hinsichtlich des Elektroformierens vorhanden. Das Materialsystem zeigt aber, auch hinsichtlich eines möglichen Aufbaus mit einem Auswahltransistor, ein hohes Potential für zukünftige ReRAM-Anwendungen.

Abstract

Conventional CMOS-technology defined by optical lithography will reach its physical limits within the next years together with technologies adopted for data storage. This work presents and combines the alternative concepts of resistively switching devices, usable as nonvolatile memory elements or switches, and nano crossbar architecture, which defer these physical limits sustainably.

The nano crossbar architecture consists of a functional component that is integrated between two perpendicularly crossing metallization lines. This configuration allows for a high integration density due to a minimal footprint of 4 F^2 (F = minimum Feature size). The basic elements are straight metallization lines with excellent scaling capability and fabricated by competitive technologies such as nano imprint lithography.

The functional component can be composed of reversibly switching TiO_2, which is integrated into metal/ insulator/ metal elements (MIM). This can be operated by corresponding set- and reset- voltages between at least two resistance states, which represent a logic „0“ or „1“. The state is nonvolatile and can be nondestructively determined by voltages below these programming values.

The field of application includes memory matrices, which are also named passive ReRAM (Resistive Random Access Memory), elements of the DRL (Diode-Resistor Logic) and RTL (Resistor-Transistor Logic), as well as router and multiplexer. Because of their passive properties, an active control circuitry, which is currently based upon CMOS, is necessary. For this reason, all materials and fabrication technologies are CMOS compatible.

The developed and optimized lift-off metallization in combination with electron beam direct writing is a flexible method to fabricate metallization lines with different metals and with a width of 50 nm. The fabricated devices comprise crossbar arrays with a size of 64 × 64 bit and a 30 nm thermally evaporated electrode of a Pt/ Ti double layer. These were examined in terms of ballistic charge transfer mechanisms, since the dimensions of the conductor were in the range of the electron mean free path. The experimental results could be explained by the models of Fuchs-Sondheimer and Mayadas-Shatzkes. Finally, the metal lines offered a high yield and a good scalability with low resistances per unit length.

The TiO_2 thin film was reactively sputtered or deposited by ALD (Atomic Layer Deposition). Subsequently, the electrical transfer from the insulating to the switching state, also called electroforming, was examined in detail and allowed for a reliable bipolar switching. The required operating voltages and currents of 100 · 100 nm^2 large cells are 2 V and several 100 µA,

respectively, which are appropriate values for a combination with CMOS technology. Additionally, the gained resistance ratio of more than 100 offers a good detection of the stored information. This information is nonvolatile without any degradation for more than 10^5 s, also at elevated temperatures of 85°C.

The switching speed was measured by short voltage pulses and is less than 10 ns. At the same time, it is possible to vary the value of the HRS (High Resistive State) depending on the pulse length and amplitude. The multitude of achievable states enables the development of a multi-bit storage element that increases the storage density without an increase of the technological complexity.

The interaction of adjacent functional elements was examined by programming of a set of neighboring junctions inside of an array. The subsequent readout of these elements showed no mutual influence for distances above 200 nm and the switching characteristic was consistent with that one of single elements. Each junction that was not electroformed inhibited parasitic currents in the bypasses of an array. The number of programmable bits is thus limited due to the high electroforming voltages of the examined material system.

The combination of both concepts shows the high potential of resistively switching elements in nano crossbar architecture. However, the operation of a complete array with the combination of Pt/TiO_2/Ti/Pt has to be optimized in respect of the electroforming. Nevertheless, this material system offers a high potential for future ReRAM applications, first of all in combination with a select transistor.

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für Margret und Michael

Contents

1 Introduction

The reason for the continuous success of the information and communication technology is the constant implementation of the demands for higher performance. This general interplay between demand and product leads to the self-fulfillment of Moore's law [1]. Memory is one of the essential core components for the performance of a system, which has to provide an ever higher storage density, lower access time and lower power consumption. CPUs are the other core components with comparable demands for higher circuit densities, faster operation and also lower power consumption. In both cases, this has to be achieved at minimum cost, which is contrary to increasing manufacturing expenses. Whether the question of cost or the predicted physical limits, which accompany this technology since the invention of the integrated circuit by Kilby and Noyce in 1958/59, present the end of the road map is open [2]. Although several branches like consumer electronics and partially automotive electronics, slowdown their pursuit of performance gain during the last decade, several other applications still require a performance improvement. To mention only a few of them, these are today's mobile entertainment and communication electronics with multimedia applications but also industrial control systems for the work flow of complex automatic machine tools.

Focusing on today's memory technology, this is dominated by a combination of extremely fast SRAM (Static Random Access Memory), fast DRAM (Dynamic Random Access Memory) and nonvolatile hard disk drives or flash memory. This hierarchy is necessary to circumvent the respective disadvantages of these components. In short, fast memory devices are expensive, comparably large and volatile, whereas nonvolatile storage devices are slow. In general, to be a competitor for future memory and storage applications, a device has to merge several advantageous properties. These are high operating speed, high scalability, nonvolatility, low power consumption and high endurance. Additional aspects are a good compatibility with Si technology and high volume production at minimum cost. Today's emerging alternatives focus on nonvolatile systems like MRAM (Magnetic RAM) [3, 4], FeRAM (Ferroelectric RAM) [5, 6], and PCRAM (Phase Change RAM) [7]. To this day, their advantages could however not prevail and replace the dominating technologies.

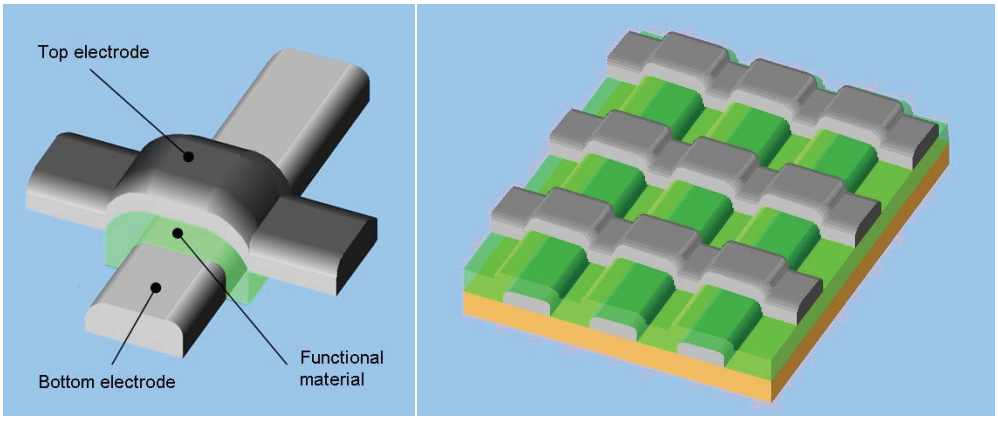
A major issue is the general technological scaling constraint, which also concerns today's approach for the arithmetic logical unit (ALU). This is based on CMOS circuits for Boolean logic, which require an extremely high accuracy when reaching technology nodes beyond 10 nm. To minimize deviations of operation parameters like the voltage threshold within a reasonable limit, the manufacturing precision has to be within the range of a few angstroms. Even if this could be technologically accomplished, the fabrication costs would increase dramatically. This fact concerns also memories that require one or more transistors, for example.

A general approach is the development of alternatives beyond CMOS technology. However, bottom up technologies like nano-tubes establishing FETs (field effect transistors) are still a challenge in regard of a selective alignment, although theoretical considerations include this

technique by an alternative fabrication method [8-11]. In other respects, functional molecules offer interesting nonlinear properties but their arrangement and combination to logical structures is still an unsolved task [12, 13]. This applies accordingly for a controlled contacting by a physical interface between molecules and the outside world.

As bottom up technologies are a long-term challenge, alternative top down technologies constitute the short- and mid-term opportunity, because at present, solid state materials still offer an ease of operation. In this context, nano crossbar architecture in combination with a resistively switching material is a promising candidate for future memory and logic applications. The switch or memory element itself is a metal/insulator/metal (MIM) stack as illustrated in figure 1.1 (a). This creates a profoundly scalable device with two terminals where the signals for the programming as well as the reading are applied. Considering two perpendicularly arranged metal lines sandwiching the functional layer, each crosspoint junction creates a functional element. The extension to a set of parallel metal lines creates finally a crossbar array as shown in figure 1.1 (b) [14]. Wires in the form of straight lines and with a parallel alignment are easy to fabricate. For this reason, they provide a high potential for downscaling and an appropriate device density. Furthermore it enables the application of novel fabrication techniques like nano imprint lithography or interference lithography, which are both low cost technologies [15-17].

A functional material switches or stores information reversibly in the form of different resistance values. The resistance is adjusted by a voltage signal that exceeds a certain threshold for the writing or erasing. This state is typically nonvolatile and can be read nondestructively with any voltage below the threshold voltage. In addition to the memory application, named ReRAM (Resistive Random Access Memory), an implementation of computing modules with diode resistor logic, routers or multiplexers is possible [18-21]. A future intention could also be the implementation of artificial intelligence by the use of a learning system on the basis of neural networks. This application is discussed since decades and becomes interesting again as the device density and operation characteristics reach those of the human cortex [22, 23]. However,



(a) (b)

Figure 1.1: (a) MIM stack of a crosspoint junction. (b) Arrangement of a crossbar array by a set of parallel electrodes.

these applications depend on a dexterous assembly of the array as well as an appropriate functionality of the used material system. Multitude resistively switching materials were investigated within the last decades with different operational parameters and switching mechanisms, making them more or less suitable for memory or logic applications [24-26]. However, these investigations are mostly related to single memory elements and were only theoretically transferred into passive arrays [27]. A practical investigation of the crossbar architecture is often missing.

This study receives the integration of resistively switching TiO_2 into nano crossbar arrays with Ti/Pt metallization lines. The objectives for the accomplishment of this task are:

- An implementation of a flexible method for the patterning of nano sized metallization lines and crossbar arrays with various electrode materials. The technique of the pattern fabrication is at least suitable for a BEoL-process (Back End of Line).
- The composition of a CMOS compatible material system consisting of a functional material and corresponding electrodes showing reliable resistive switching characteristics.
- An investigation of the metal lines concerning their suitability for nano crossbar architecture and a future downscaling of their dimensions.
- The fundamental parameterization of the resistance switching in fabricated crosspoint junctions in consideration of its suitability for a CMOS control circuitry. Additionally, the examination of the switching performance with respect to the switching speed.
- An investigation of the switching properties of TiO_2 in nano crosspoint junctions and arrays concerning the future application as ReRAM element.

After a brief summary of today's memory technology, chapter 2 provides the basics and the physical model about the resistance switching in TiO_2. Finally, a short outline of potential future applications is given. Chapter 3 introduces the relevant fabrication methods, particularly the electron beam direct writing, concerning the presented devices, and describes their features in context with nano crossbar structures. Analytical methods like SEM (Scanning Electron Microscopy), AFM (Atomic Force Microscopy) and electrical measurement setups are described in chapter 4, related to their properties within the given context. The electrical results for nano crossbar arrays and devices are described in chapter 5, which focuses on the properties of nano wires. Chapter 6 presents the combination of these devices with the incorporated TiO_2. This contains the description of the initial electroforming process and the electrical parameterization of TiO_2. In chapter 7, the electrical characterization is concluded with the examination of the devices considering practical future applications like switching properties by short pulses and characteristics of a passive array. Finally, an outlook is given that addresses future tasks and open challenges, which correspond to the use of the present structures as templates for new materials or as initial position for structural investigations. Additionally, considerations about the use of TiO_2 as functional material are presented.

2 Fundamentals

The following chapter gives a basic introduction on resistance switching of solid state materials, in particular TiO_2, and the nano crossbar architecture. This is motivated by the limitation of the present memory devices, which serve as a benchmark for this novel concept. Also alternative and new concepts like FeRAM, PCRAM and MRAM cannot circumvent some of these limitations. Additionally, the conduction mechanism of nano sized metal lines is described in consideration of their application in nano crossbar arrays. Finally, a brief overview is given for possible future logic applications to demonstrate the potential of this architecture.

2.1 Current memory devices

Today's memory systems consist of a hierarchy of several devices that have to meet different requirements which cannot be incorporated into one single device. To support the CPU or ALU with commands and data, a very fast memory access has to be guaranteed. This is done by SRAM, which consists of a set of six transistors per cell that operate as a flip-flop-latch. The direct implementation in CMOS, mostly embedded in the logic units within an integrated circuit, allows for a constant progress in performance. But for this reason, it provides no potential as a 'beyond CMOS' technology. Furthermore, SRAM offers a low memory density and is very expensive in regard of cost per bit. From an economical point of view, the memory size is limited, and it is only used as cache memory. Additionally, this technology needs a permanent electricity supply to maintain the stored information.

DRAM is about one order of magnitude slower in time than SRAM and would become a bottleneck directly supporting the CPU. However, its cell area is essentially smaller, and its costs per bit are considerably lower. It consists of a select transistor and a storage capacitor representing the information by being charged or uncharged. Due to its high performance and its comparable large memory capacity, DRAM represents the primary memory and is a driving part for the performance in a computer system. With nearly constant or even decreasing costs for complete modules the storage capacity has been increased by a factor of four every 3 to 4 years. Despite these advantages DRAM is still too expensive for mass storage applications. Furthermore, it also needs a permanent supply of electrical power to compensate the charge leakage. Finally, its scalability is limited by the capacitor, which has to provide enough capacity to store a detectable amount of charge. Although, this can be increased by high-*k* materials or advanced capacitor configurations, it is limited by complexity and costs [28]. Finally, the resulting power dissipation of these volatile memories is not economic and efficient, in particular for mobile applications. Additionally, a loss of information in case of an interruption or defect in the power supply is not acceptable.

Nonvolatile rewritable systems like hard disk drives or NAND- and NOR-flash memory fulfill this demand. They are used as secondary storage offering a high capacity but including a

long access time. For example, recent hard disk drives achieve a storage size of 2 TByte, which increases around one order of magnitude every five years. The external transfer rate is several hundred MByte · s^{-1}. However, due to the mechanical setup, an additional access time of several milliseconds is needed, and possible mechanical malfunctions are disadvantageous.

Finally, flash memory presents the dominant nonvolatile solid state storage system offering a fast read access. However, the write access is comparably slow, and the degeneration of the isolating oxide during the erase process results in low durability.

Table 2.1 summarizes the specific values of the fully electronic baseline technologies as a benchmark for competing devices [29]. In general, physical problems will occur caused by a continuous down scaling of the devices. These have to be avoided by more complex structures and materials. But the complexity will result in a demand for advanced fabrication routes and tools, which is directly related to lithography tools that have to become more accurate to obtain higher resolutions. This results subsequently in an increase of fabrication costs, which cannot be paid off by the gained memory/storage density, leading to an extremely high pricing for devices.

Table 2.1: Today's and projected values for 2022 of baseline technologies of memory and storage devices extracted from the ITRS 2007 edition for emerging research devices [29].

		DRAM		SRAM	Floating Gate	
		Stand alone	Embedded		NOR	NAND
		Charge on capacitor		Interlocked state of logic gates	Charge on floating gate	
Cell elements		1T 1C		6T	1T	
Feature size F [nm]	2007	68	90	65	90	90
	2022	12	25	13	18	18
Cell Area F^2	2007	6	12	140	10	5
	2022	6	12	140	10	5
Read Time	2007	<10 ns	1 ns	0.3 ns	10 ns	50 ns
	2022	<10 ns	0.2 ns	70 ps	2 ns	10 ns
W/E time	2007	<10 ns	0.7 ns	0.3 ns	1 us 10 ms	1 us 0.1 ms
	2022	<10 ns	0.2 ns	70 ps	1 us 10 ms	1 us 0.1 ms
Retention time	2007	64 ms	64 ms	--	>10 y	>10 y
	2022	64 ms	64 ms	--	>10 y	>10 y
Write Cycles	2007	$>3\cdot10^{16}$	$>3\cdot10^{16}$	$>3\cdot10^{16}$	$>10^5$	$>10^5$
	2022	$>3\cdot10^{16}$	$>3\cdot10^{16}$	$>3\cdot10^{16}$	$>10^5$	$>10^5$
Write operating voltage [V]	2007	2.5	2.5	1.1	12	15
	2022	1.5	1.5	0.7	12	15
Read operating voltage [V]	2007	2	2	1.1	2	2
	2022	1.5	1.5	0.7	1.1	1.1
Write Energy [J/bit]	2007	$5\cdot10^{-15}$	$5\cdot10^{-15}$	$7\cdot10^{-16}$	$>10^{-14}$	$>10^{-14}$
	2022	$2\cdot10^{-15}$	$2\cdot10^{-15}$	$2\cdot10^{-17}$	$>10^{-15}$	$>10^{-15}$

These occurring challenges raise the demand for alternative memory concepts combining high performance with nonvolatility and a method to apply low cost technology.

2.2 Alternative memory concepts

At the moment, three arising alternatives are in the prototype stage or are already in production. These are FeRAM, MRAM, and PCRAM. ReRAM will compete with them, because these four concepts offer nonvolatility and belong to the solid state technology providing an alternative; at least for flash memory. The following table 2.2 describes their characteristics to give an overview over their advantages and disadvantages. Subsequently, they are briefly described and compared with baseline technologies such as DRAM and flash memory, illuminating the emerging demands for ReRAM.

Table 2.2: Today's and projected values for 2022 of prototypical technologies of memory and storage devices extracted from the ITRS 2007 edition for emerging research devices [29].

	FeRAM Remanent polarization on a ferroelectric capacitor		MRAM Magnetization of ferromagnetic layer		PCRAM Reversibly changing amorphous and crystalline phases	
Cell elements	1T 1C		1T 1R		1T1R or 1D1R	
Considered year	2007	2022	2007	2022	2007	2022
Feature size F [nm]	180	65	90	22	65	18
Cell Area F^2	22	12	20	16	4.8	4.7
Read Time	45 ns	<20 ns	20 ns	<0.5 ns	60 ns	<60 ns
W/E time	10 ns	1 ns	20 ns	<0.5 ns	50/120 ns	<50 ns
Retention time	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
Write Cycles	10^{14}	$>10^{16}$	$>3\cdot10^{16}$	$>10^{16}$	10^{8}	10^{15}
Write operating voltage [V]	0.9 – 3.3	0.7 - 1	1.5	<1.5	3	<3
Read operating voltage [V]	0.9 – 3.3	0.7 - 1	1.5	<1.8	3	<3
Write Energy [J/bit]	$3\cdot10^{-14}$	$5\cdot10^{-15}$	$7\cdot10^{-11}$	$2\cdot10^{-11}$	$5\cdot10^{-12}$	$<10^{-13}$

2.2.1 MRAM concept

An active MRAM cell consists of a select transistor and the magnetic memory element as illustrated in figure 2.1. The latter is a stack of two ferromagnetic layers that sandwich a thin insulating film [3]. One layer has a pinned ferromagnetic polarity, whereas the other one can be changed by an external field. Therefore, the element is positioned at the intersection of a bit line and a write word line. Both wires induce a directed and turning magnetic field that traces the magnetic axis of the free layer over the hard direction into the opposite direction. However, high currents are necessary to provide the writing field, which represents a disadvantage of this technology.

If both ferromagnetic layers have a parallel polarity, the electrons can tunnel easily through the oxide layer due to the magnetic tunneling effect, and the element is in the LRS (Low Resistive State). On the other hand, if they are aligned anti-parallel, tunneling is suppressed, and the element is in the HRS (High Resistive State). This can be determined by the current response through the bit line once the select transistor is opened by the read word line.

Compared to flash memory, writing and erasing is essentially faster. The endurance is comparable with DRAM, the operation times are higher but the write voltage is lower. The larger cell area is a disadvantage as well as the high programming currents, which also increases the write energy for more than two orders of magnitude.

2.2.2 PCRAM concept

Phase-Change RAM has a comparable architecture to DRAM [30]. Each cell consists of a select transistor and a memory element, whereby these cells are arranged in a matrix of word and bit lines for addressing and operation. This is schematically described in figure 2.2. The key component is the memory element, which contains chalcogenide compounds. In detail, this is an element of the sixteenth group (S, Se, and Te) in combination with Ge, Sb or As creating a glassy solid state body. It can adopt a crystalline or amorphous phase creating a LRS or HRS. For this reason, the material is connected by two metal electrodes, which are used to induce a time- and amplitude- controlled current pulse. A current pulse with a longer duration and a lower level heats up the material above the crystallization temperature and induces crystallization. In contrast, a fast pulse with a high current also generates enough heat to exceed the crystallization temperature, but due to the short duration an under-cooled amorphous state is generated. This effect is also used for rewriteable CD or DVD disks, where the corresponding state is determined optically by the reflectivity.

The information of the PCRAM is determined by a small voltage that generates a current response, which provids information about the state without heating up the element. Compared to flash memory, PCRAM provides faster programming sequences; however, it needs a higher write energy and thereby increase the energy consumption. On the other hand, the

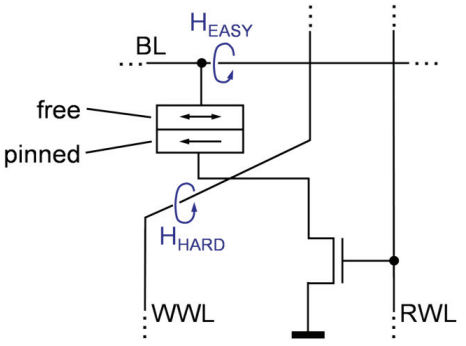


Figure 2.1: Scheme of a MRAM storage cell.

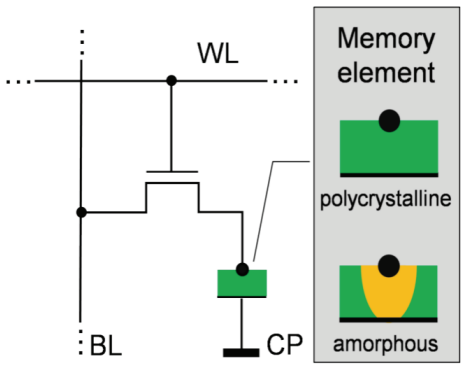


Figure 2.2: Scheme of a PCRAM storage cell.

operating voltages are lower, and the endurance during operation is essentially higher. However, the given and predicted values are not meeting those of DRAM.

2.2.3 FeRAM concept

In general, the setup of FeRAM is comparable to DRAM, because each memory cell consists of an access transistor and a ferroelectric capacitor [31]. Here, the information is not stored by a charge but by the remanent polarization P of the incorporated ferroelectric film. This can be programmed by an electric field E that is applied at the capacitor. The $P(E)$ nature of a ferroelectric material is a hysteresis with a positive and a negative remanent polarization P_r, which is nonvolatile in the case of an absent electric field.

Depending on the voltage, the polarization is either switched into the positive or negative direction. If the polarization changes due to the voltage pulse, a high amount of charge is shifted by a current flow. If the polarization already has the intended direction, only a small amount of charge is shifted due to the dielectric response of the ferroelectric material. The information can be read by the voltage over a capacitance divider of the ferroelectric and the bit-line capacitance. Depending on the polarization state this read voltage is above or below a reference voltage and can be distinguished to define the stored state of the FeRAM element.

FeRAM offers low write and erase times and an essentially higher endurance than flash memory. Apart from a lower operating voltage, the currents are also lower, resulting in a comparably low write energy, which is essentially smaller than in MRAM. However, the absolute cell area is also larger than MRAM and its scalability is limited. Additionally, the memory is indeed nonvolatile, but the read-out is destructive.

In summary, the last examples are realized in CMOS technology combined with alternative materials and require a select transistor. Therefore, their technical down scaling potential is limited, and their advantages focus mainly on the nonvolatility.

2.3 Physics of nanometer metal lines for crossbar architecture

Straight nano sized metal lines are the basic elements of the crossbar architecture. The following section discusses the physics of conductors in the nanometer regime, where the geometrical dimensions become comparable with the mean free path of the electrons. Typically, the reduction of the lateral dimensions leads to a corresponding increase of the resistance per wire length, but for the crossbar array architecture, the required length for a functional element is proportional to the wire width. As a result, the conductor resistance per cell should be constant. However, material properties in this dimensional range tend to deviate from those of bulk materials due to scattering effects along surfaces and interfaces. This additional increase of nano metal line resistivity can result in a disadvantageous ratio of the voltage drop between the functional element and its corresponding conductor element [32].

With several simplifications a metal body is an electrical linear device, responding with a current I proportional to the voltage V applied at the body. The resistance R is the proportionality

factor, which is normally supposed to be constant according to Ohm's law $R = V / I$. By normalizing voltage and current by the geometrical parameters, one obtains the resistance depending on the physical dimensions of the body with the length l, the thickness t and the width w. Here, l is parallel to the applied electric field E resulting in $V = E \cdot l$, and $w \cdot t = A$, which is the area passed by the current $I = J \cdot A$. The electric field E over the current density J is defined as the electrical resistivity ρ.

$$R = \frac{E}{J} \cdot \frac{l}{t \cdot w} = \rho \cdot \frac{l}{t \cdot w} \tag{2.1}$$

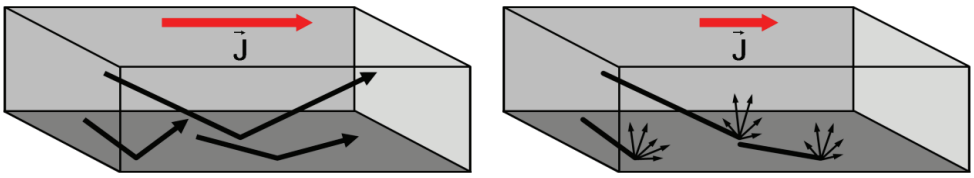
The mean free path of an electron λ_{MFP} indicates the medial distance that can be covered between two subsequent interactions with the surrounding matter. This effect of isotropic scattering at phonons or point defects is included in the resistivity ρ, which is therefore material specific. Conduction within an infinitely wide body with a monocrystalline texture is described by the conductivity σ_0, and anisotropic electrical properties, which split σ_0 into respective matrix elements, are neglected for the used materials. So, any kind of transport is characterized by the interaction between the charge carriers, here the electrons, and the matter. Beneath this material dependent conductivity σ_0 two additional scattering effects occur if any physical dimension of the conductor (here, l, w and t) is reduced to the range of the mean free path. Some values for the mean free path taken from literature are given in table 2.3.

Table 2.3: Ideal values for the mean free path of electrodes in metal conductors

Material	Mean free path	Literature
Ag	52 nm	[33]
Cu	39 nm	[33]
Ti	29 nm	[34]
Pt	23 nm	[35]
Al	15 nm	[33]

2.3.1 Fuchs and Sondheimer model

Fuchs developed his well-known size-effect theory, after he observed a strong increase of the resistivity in alkali metal thin films by decreasing the film thickness [36]. If the body is limited by surfaces, electrons are reflected back into the material. This reflection can be partially specular as illustrated in figure 2.3 (a) or partially diffuse according to figure 2.3 (b). The ratio between both effects depends on the properties of the involved surface. A diffuse reflection reduces the conductivity of the material in contrast to a specular reflection. The physical interpretation for the latter is that electrons retain their momentum parallel to the field, and their contribution to the effective current is unchanged. For a diffuse reflection, the electrons loose



(a) (b)

Figure 2.3: (a) Specular reflection of electrons at a conductor surfaces corresponding to a reflection parameter p = 1. (b) Diffuse reflection of electrons at a conductor surface corresponding to a reflection parameter p << 1.

part or all of their impulse in field direction. As a result the total current decreases. This effect is described statistically by the parameter p. In the case that all charge carriers are reflected specularly, $p = 1$. It becomes 0 if all electrons are, in contrast, reflected in a diffuse way. The diffuse reflection correlates to the atomic and not with the mesoscopic roughness of a surface or interface [37]. Therefore, it cannot be determined by AFM scans, for example.

Provided that the distance between two opposite surfaces of a body, here the thickness of the film t_f, is small in comparison to the mean free path λ_{MFP} of the electrons, the fraction of the resistivity due to surface scattering becomes relevant in regard of the bulk resistivity ρ_0. For thin films Fuchs describes the resistivity increase by

$$\rho = \rho_0 \cdot \left(1 - \frac{3\lambda_{MFP}}{2t_f}(1-p)\int_1^{\infty}\left(\frac{1}{u^3}-\frac{1}{u^5}\right)\frac{1-e^{-\frac{t_f}{\lambda_{MFP}}u}}{1-p\cdot e^{-\frac{t_f}{\lambda_{MFP}}u}}du \right)^{-1} . \tag{2.2}$$

The origin of u is a simplifying substitution of the relevant polar coordinate θ by $u = 1/cos\theta$ within its borders between 0 and π/2.

For an absolute diffuse reflection with $p = 0$, Steinhögl et al. described the effective resistivity by the statistical distribution of the electron impulse over the hemisphere within the solid state body by a complex analytical function, given as equation 2.3 [38].

$$\left.\frac{\rho_0}{\rho}\right|_{p=0} = f(\lambda,w,t) = 1 - \frac{6}{4\pi\cdot tw}\int_0^w\int_0^t\int_{-\arctan\left(\frac{y}{x}\right)}^{\arctan\left(\frac{t-y}{x}\right)}\int_0^{\pi}\sin(\theta)\cos^2(\varphi)\left[1-e^{-\frac{x}{\lambda\cdot sin(\theta)cos(\varphi)}}\right]d\theta\theta\varphi dydx$$
$$-\frac{6}{4\pi\cdot tw}\int_0^w\int_0^t\int_{-\arctan\left(\frac{x}{t-y}\right)}^{\arctan\left(\frac{w-x}{t-y}\right)}\int_0^{\pi}\sin(\theta)\cos^2(\varphi)\left[1-e^{-\frac{t-y}{\lambda\cdot\sin(\theta)\cos(\varphi)}}\right]d\theta\theta\varphi dydx \tag{2.3}$$

This equation applies for rectangular conductor profiles with the thickness t_{cd} and the width w_{cd}. If the reflection parameter p becomes larger than 0, equation 2.3 is included into the series expansion

$$\left.\frac{\rho}{\rho_0}\right|_{p>0} = (1-p)^2\sum_{k=1}^{\infty}k\cdot p^{k-1}\cdot\left.\frac{\rho_0}{\rho}\left(\lambda/k\right)\right|_{p=0} . \tag{2.4}$$

This equation as well as equation 2.3 are analytically complete and describe no approximation [39]. The application of this detailed and precise mathematical description on conductors of nano crossbar arrays presents a high effort concerning computing time. Additionally, variations of the conductor shape and size do not accommodate the precision of the equation. So, feasible approximations were given by Sondheimer for circular and quadratic conductors with different ratios between the wire dimensions and the mean free path of electrons [39].

The cross sectional dimensions of the wires within the in the following described nano crossbar arrays are in the range of the mean free path of electrons for bulk materials, given in table 2.3. As the ratio between width and thickness of the fabricated wires changed in the range from nearly 1 to around 17, the given approximations for square-shaped conductors induce certain deviations. Steinhögl et al. developed a simple approximation for rectangular copper wires depending on the circumference c_{cd} and the cross sectional area of a conductor A_{cd} [38].

$$\frac{\rho}{\rho_0} = 1 + c_{cf}(1-p)\frac{c_{cd}}{A_{cd}}\lambda_{MFP}, \tag{2.5}$$

with the correction factor c_{cf} for the adaptation of the Steinhögl approximation to the Fuchs-Sondheimer theory. By substituting the wire dimensions w_{cd} and t_{cd} for the parameters c_{cd} and A_{cd} the approximation is

$$\frac{\rho}{\rho_0} = 1 + 2c_{cf}(1-p)\left(\frac{1}{t_{cd}} + \frac{1}{w_{cd}}\right)\lambda_{MFP}. \tag{2.6}$$

c_{cf} results in a good approximation for Cu with a value of 1.2. The effects for horizontal and vertical surfaces are supposed to be independent.

2.3.2 Mayadas and Shatzkes model

Up to now, the consideration of the resistivity referred to an isotropic, monocrystalline and dimensionally limited metal volume. However, all conductors, which are used and investigated within this context, were polycrystalline, containing grains with different sizes and textural alignments. These were separated by grain boundaries. Within each grain, the conduction responds to the above given description. For large conductor dimensions, the average distance between these interfaces is supposed to be much longer than the corresponding mean free path of an electron. Mayadas et al. deduced from observations of Al thin films that the grain

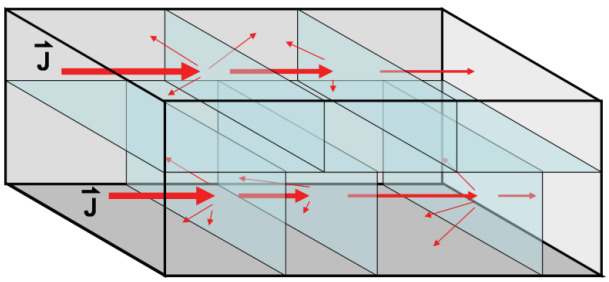


Figure 2.4: Schematic description of the model by Mayadas and Shatzkes [40]. The grain boundaries in the conductor that are aligned rectangular to the current flow represent a reflection plane.

size or the distance between grain boundaries decreases proportional with the deposited film thickness [41]. As the later presented structures had two dimensions that were in the range of several ten nanometers, it becomes obvious that the size of the grains decreases and the density of their boundaries increases correspondingly for nano conductors. The grain boundaries are interfaces that represent scattering sources for electrons. This effect is illustrated in figure 2.4. Additional defects or impurities extend the number of scattering sources [33, 42]. The higher the reflection probability for a charge carrier is, the higher is the resistivity of the conductor. Mayadas and Shatzkes extended the model from Fuchs and Sondheimer and included the effect of grain boundary reflection by the parameter R_{gb} [40]. A monocrystalline film has an $R_{gb} = 0$, whereas a full reflection results in an $R_{gb} = 1$. The relation for the resistivity is given as

$$\rho = \rho_0 \Big/ 3 \cdot \left(\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right), \tag{2.7}$$

with the scattering relation for α_{sc} and the average grain size d_g in the current direction

$$\alpha_{sc} = \frac{\lambda_{MFP}}{d_g} \cdot \frac{R_{gb}}{1 - R_{gb}} \tag{2.8}$$

In a next step, the Matthiessen relation provides the basics to combine both models. The scattering probability is inversely proportional to the relaxation time τ. Assuming that the scattering at the sidewalls and at the grain boundaries are independent from each other, the corresponding probabilities can be added to the total probability value [43]. This concludes in the simple addition of the inverse relaxation times for all participating effects. Finally, the resistivity is given by $\rho = \sigma^{-1} \sim \tau^{-1}$ leading to the conclusion

$$\rho = \rho_{ph} + \rho_{if} + \rho_{gb} + \rho_{imp} + ... \tag{2.9}$$

with fractions, caused by phonon scattering ρ_{ph}, scattering at impurities ρ_{imp} and the considered part of interface and grain boundary scattering ρ_{if} and ρ_{gb}. The assumption of the independence is only nearly valid in this context. However, a more precise description is the inequality that takes interdependence on both effects into account.

$$\rho \geq \rho_{ph} + \rho_{if} + \rho_{gb} + \rho_{imp} + ... \tag{2.10}$$

However, Steinhögl et al. assume that an acceptable accuracy is given and that the significant resistivity can be summed up [44]. This leads to an equation that contains the intrinsic resistivity ρ_0, ρ_{gb} and the horizontal as well as the vertical fraction of ρ_{if}

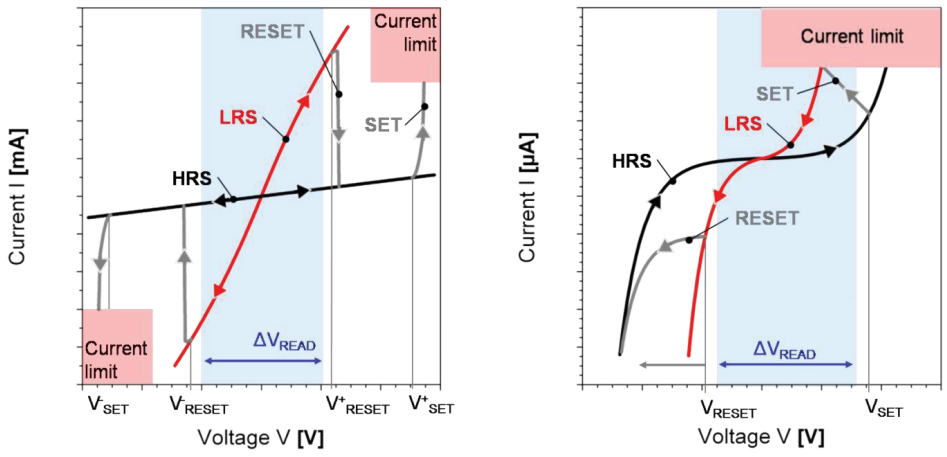
$$\rho = \rho_{if}^{(h)} + \rho_{if}^{(v)} + \rho_{gb} \tag{2.11}$$

$$\frac{\rho}{\rho_0} = 2C \cdot \lambda_0 (1 - p)\left(\frac{1}{t} + \frac{1}{w}\right) + \frac{1}{1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)} \quad . \tag{2.12}$$

The validity of this relation for a combination of both effects is also shown by Durkan et al., but a relation between the decrease of the mean grain size and the structural dimension must be taken into account [45].

2.4 Resistance switching for ReRAM

Two different switching effects were observed for TiO_2 as well as for several other materials [46]. The first one is the unipolar switching that can be controlled by a single polarity to switch reversibly between a HRS and a LRS. To distinguish between a set- and a reset-process a current limit and certain voltage amplitude are needed. In the first case, the current increases abruptly at the set-voltage as shown in figure 2.5 (a). Therefore it has to be limited by a current compliance to prevent an immediate reset or a thermal breakdown. The latter case is operated with a voltage below the set- and above the reset-value at which the current decreases drastically while switching into the OFF-state. Typically, both polarities can be used for the unipolar switching as illustrated in figure 2.5 (a), why this mechanism is rather nonpolar than unipolar. The nature of this mechanism offers the advantage of an operation with a single polarity, which simplifies the triggering for an external control circuit considerably. The reason for the switching is explained by the fuse-antifuse effect. This assumes the formation or rupture of a conducting path due to an electric field and thermal impact. The surrounding material is insulating as well as the material in the disrupted state. Several transition metal oxides besides TiO_2, like NiO and Nb_2O_5 exhibit unipolar switching [24, 47-51]. Nevertheless, the observed currents in TiO_2 are in the mA range, which is not only an issue with regard to low power consumption. The required currents are often not directly scaling with the device size and result in accordingly high current densities. The outcome is an overstress of the device electrodes, which is demonstrated for nano wires in chapter 7.



(a) (b)

Figure 2.5: (a) Schematic of a resistive switching curve for unipolar and (b) bipolar switching. The black curve indicates the HRS and the red one the LRS. Please note the different scale of the current axis.

The second and for this study more important effect is the bipolar switching, which is shown in figure 2.5 (b). This graph presents a typical current response for a bipolar double voltage sweep. In this case, different polarities are used for writing and erasing. This means for the given example that a set-process is always performed by exceeding a positive threshold voltage and that a reset-process is triggered by the exceeding of a negative threshold voltage. The asymmetry of the switching curve is normally caused by an asymmetry of the memory element. This can be caused by different electrode materials for the top and bottom electrode or a directed treatment during the electroforming process.

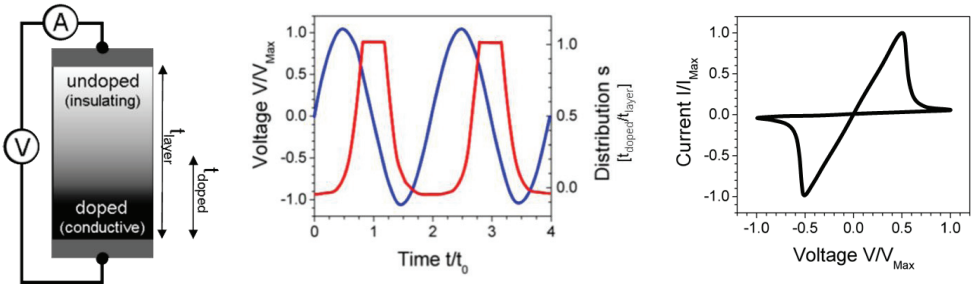
The virgin state of the TiO_2 is in general highly insulating, and an electroforming step has to be applied, which transfers the material into a switchable state (for details see chapter 5). The electroforming is mandatory for both switching mechanisms. However, comparing the respective ones, unipolar switching is generated by a high current compliance during the electroforming and bipolar switching by a lower current limit. These were at least one to two orders of magnitude lower in the latter case. The result was amongst others a lower operation current.

In conclusion, bipolar switching in TiO_2 revealed the advantage of lower operation currents and a lower susceptibility concerning deviations of the switching signal, which means in detail V_{reset}, V_{set} and I_{reset}. As a result, this study focused on bipolar switching because of its lower power consumption and lower operating currents. The former is a general demand whereas the latter yielded an essentially lower failure rate in the nano metallization lines.

2.5 Bipolar resistance switching in TiO_2

Since the last decade and recently, the interest in resistively switching materials increased considerably, last but not least, due to bridging the gap between resistance switching and the memristor, described by Chua in 1971 [52]. He extended his description finally to memristive systems in 1976 and gave examples like thermistors, nerve axon membranes described by the Hodgkin-Huxley model and discharge tubes [53]. Nevertheless, resistively switching thin films were never classified in this context for decades.

Strukov and the group of Williams did so in 2008 and described the resistance switching of transition metal oxides in the framework of the memristor model [54]. The general relation between voltage and current, that is $v = R(s) \cdot i$, persists, which counts most notably for the absent phase-difference between current and voltage. This becomes apparent by the mutual zero-point crossing, which is a fundamental criterion for this model. The occurring memristance depending on the state s concerns merely the resistance R itself. The proposed system is a coupling of solid-state electronic and ionic transport, whereby the ionic fraction acts as dopant in a semiconducting material, which is illustrated in figure 2.6. Their position can be controlled by an external electric field, which can rearrange their distribution in the material. The result is a simplified serial connection of a volume with a higher and one with a lower or no dopant concentration as illustrated in figure 2.6 (a). So, the state variable s depends accordingly on the



(a) (b) (c)

Figure 2.6: (a) Scheme of the doping distribution in a MIM stack [54]. The distribution $s = t_{doped}/t_{layer}$. (b) Dopant distribution depending on the applied voltage [54]. (c) The corresponding I(V) characteristic [54].

fraction of the occupied volume and gains values between 0 and 1. If the complete film with the thickness t_{film} is doped, the resistance reaches its minimum R_{ON}. An accumulation of the dopant in a fraction of the volume creates, however, a high R_{OFF} caused by the otherwise undoped fraction. These simple assumptions lead to an approach for the memristance of coupled ionic and electronic charge transport. For small voltages the electronic transport dominates the current response, which can be simply described by R_{ON} and R_{OFF}. However, this depends on the distribution of the ions in the material. The ionic transport, which is forced by higher voltages, affects the occurring resistance, which is given as [54]

$$R(s) = R(q,t) = R_{OFF}\left(1 - \frac{\mu_{ion} R_{ON}}{t_{film}^2} q(t)\right). \tag{2.13}$$

R_{ON} and R_{OFF} are simplified phenomenological and static values depending on the material system. The memristive nature is described by the ion mobility μ_{ion} and controlled by the time-dependent charge influence $q(t)$. The characteristic loop of the current over the voltage is generated by a phase shift of the resistance or the dopant distribution, respectively, which is shown in figure 2.6 (b). The resulting $I(V)$ characteristic is presented in figure 2.6 (c). Please note that the ions are assumed to move along the electric field as long as a voltage with a specific polarity is applied, yielding an increasing or decreasing resistance. The state can be modulated by the applied amplitude and frequency of the signal, resulting in a continuous adjustment of the conductivity. Appropriate parameters allow for a resistance decrease while the amplitude of the voltage increases and creates a negative differential resistance. The occurrence of a threshold voltage in combination with a nearly abrupt state exchange is explained by Strukov as a result of the ionic drift in high electric fields [54-56]. This leads to the causal nonlinearity. The devices that are tested in this context consist of TiO_2/TiO_{2-x} sandwiched between two Pt electrodes. Positively charged oxygen vacancies act as dopant, which switch the device by their distribution within the material. Typically, pristine TiO_2 is a highly insulating material. A reduction process, called electroforming, transfers TiO_2 into rather semiconducting TiO_{2-x} and generates these oxygen vacancies. Therefore, the material is classified as an anion-migration system [46, 57, 58].

(a) (b)

Figure 2.7: Barrier modulation by oxygen accumulation along the interface between (a) HRS corresponding to a wide barrier and (b) LRS corresponding to a narrow barrier [59].

Zhirnov seizes the resistance switching of TiO_2 by its doping with oxygen vacancies [59]. Here, the switching is however not explained by a bulk but by an interface effect. If the oxygen atom is removed from its lattice position and the uncompensated valence of the nearby Ti atom creates an oxygen vacancy, the material becomes semi-conductive. An electric field biases the vacancies in the material, which is assumed to be constantly reduced. As a result they are pushed towards or pulled away from the metal electrode by the electric field. The Pt/TiO_2 interface between the metal electrode and the binary oxide bulk represents a Schottky-barrier. The consequence of the field and the attending shift of the vacancies is an expansion or shrinkage of this barrier as explained in figure 2.7. The current flow becomes unidirectional if the barrier expands and minimizes the tunneling probability. Vice versa, the current is bidirectional and increases if the barrier width decreases. A bidirectional voltage sweep with a correspondingly high voltage leads therefore to a hysteretic current response by changing the Schottky barrier twice within a loop. This mechanism was also assumed for TiO_2 by Jameson et al. [60].

Yang combines the presented memristor model with the influence of the oxygen/metal interface [61]. Therefore, a double layer of TiO_2 and reduced TiO_{2-x} is incorporated into a Pt electrode assembly, whereas the TiO_{2-x}/Pt interface is assumed to be ohmic. The already introduced memristor model serves as a general explanation of the resistance switching. Ionic transport refers to positively charged oxygen vacancies in TiO_2, generated by the source volume of already reduced TiO_{2-x}. Physically attractive paths, which might be grain boundaries, for example, are chemically reduced, resulting in an essentially lower resistivity. When these paths penetrate the thin film towards the opposite Pt electrode, oxygen vacancies accumulate along the TiO_2/Pt interface. As these act as an n-type dopant, they can modulate the barrier generated by the interface [62]. That means in detail that an accumulation along the interface reduces the barrier thickness and allows for an electron tunneling as described by Zhirnov. A field, which is directed opposite, reduces the dopant fraction and extends the barrier width. The subsequent switching is bipolar, and its direction depends directly on the composition of the device. For the LRS an electron tunneling process was assumed, as the current characteristic showed an exponential voltage dependency for both polarities.

A more detailed model about the generation of a conductive path by oxygen vacancies was described by Jeong et al. [58]. He examined a symmetric stack of Pt/TiO_2/Pt with regard to the electroforming process in vacuum and ambient atmosphere. An oxygen gas accumulation at the

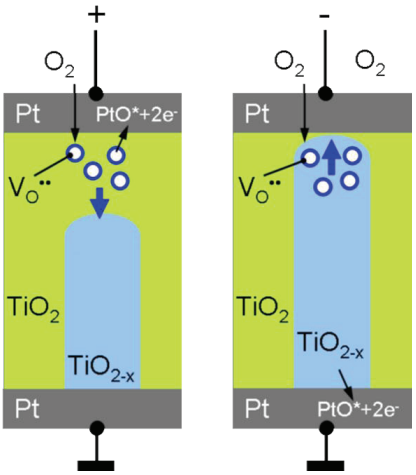


Figure 2.8: Two step electroforming process with changing polarities [58]

anode during the electroforming is interpreted as a hint for the source of the oxygen vacancies. This mechanism is also described by Yang et al. [57]. However, Jeong assumed that the interface between the TiO_2 and the Pt electrode generates the dopant. The chemisorption of the oxygen by Pt results in PtO^* and the dissipation of electrons resulted in oxygen vacancies. Depending on the polarity during the forming step the anode faced the surface or the substrate of the sample. This case is illustrated in figure 2.8. So, the oxygen can leave as gas into the atmosphere or is accumulated in the vicinity of the electrode or in the electrode itself [63]. Due to the applied field and the concentration gradient the positively charged vacancies drift towards the cathode. There they start to establish a conductive path consisting of reduced TiO_{2-x}, growing towards the anode. Additionally, the accumulation of oxygen vacancies at the bottom electrode interface reduces the height of the corresponding Schottky barrier. In contrast, a balancing exchange of oxygen at the top electrode yields an oxidation of the Ti valences at this interface. As a result the conducting path cannot connect the electrodes due to a lack of vacancies along the top interface increasing the corresponding Schottky-barrier. An opposite polarity creates either oxygen vacancies, which close the path, or shifts the existing vacancies towards the upper electrode. This serves as an explanation for the necessity of a bipolar electroforming process, which needs two sweeps with different polarities to switch to the ON- state. As an oxidation near the top electrode surface can be excluded in a vacuum only a single electroforming step should be sufficient. Experimental investigations support this assumption. The switching itself corresponds to the modulation of the Schottky-barrier height by the density of oxygen vacancies at the metal/oxide interface. Here, it was also considered and observed that this is related to only one electrode. The other one has to be passive and ohmic in the ideal case. However, it was possible to activate both electrodes, resulting in the superposition of two opponent switching characteristics as described by Jameson et al. [60].

Finally, a different effect that belongs to the cation-migration processes, which is also possible for transition metal oxides like TiO_2, should be briefly mentioned. Tsunoda et al.

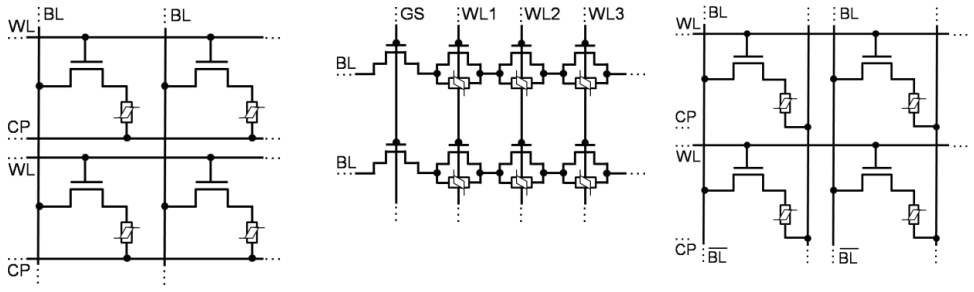
showed bipolar resistance switching in TiO_2 deposited on a Pt bottom electrode, but equipped with an Ag top electrode [64, 65]. In contrast to the system that is presented within this study, they used polycrystalline TiO_2 serving as matrix material. The Ag top electrode is a cation source for a metallic filament propagating from the cathode to the anode. The current response showed two abrupt steps for the set- and the reset-transition over more than 6 orders of magnitude. The threshold voltages were small and, as well as the whole characteristic, comparable to programmable metallization cells [66]. The nature of the LRS is metallic, which supports this theory, and not exponential, which could indicate a tunneling mechanism due to a Schottky barrier in an anion-migration mechanism. The same applies probably for Cu, which was used in combination with TiO_2 by Watanabe et al. [67]. Here, the switching was explained by a high carbon concentration due to residual precursor fractions, but updated considerations about the influence of Cu suggest the formation and decomposition of a filament [68].

In conclusion, the anion migration based mechanism of a chemical reduction of TiO_2 to TiO_{2-x} creating a conductive path is a seriously discussed model. The switching process is explained by the modulation of the Schottky-barrier due to the enhancement or depletion of mobile oxygen vacancies.

2.6 Concepts for resistive switching applications

2.6.1 Active ReRAM

An evident concept for the implementation of resistively switching MIM structures is an active RAM. Every memory element is accessed or isolated by a select transistor. So, the arrangement is a 1T1R cell. The setup of a cell depends on the distinguished concepts of NOR and NAND as shown in figure 2.9. In the first case, the 1T1R cells are composed in parallel, whereas each transistor is operated by the potentials of the bit line and the word line (gate). Source and drain are in series with the resistive switching MIM structure. This is on the other side connected with the plate line. So far the structure is comparable with DRAM and FeRAM. However, the plate line can be charged with ground or V_{DD} to invert the voltage drop over the resistance for



(a) (b) (c)

Figure 2.9: Circuit diagram for an active ReRAM in (a) NOR array, (b) NAND array, and (c) AND array with resistive switching MIM structures for memory applications.

the required bipolar control signal. As the plate line is also controlled by a driver, its dimension limits the number of columns in a memory matrix. The reason is given by degrading voltage drop at cells with increasing distance to the plate line driver.

In the NAND architecture a set of n cells is connected in series, which is comparable with the NAND-flash memory or chain FeRAM [69]. However, the switchable resistance is in parallel to the source/drain of the transistor. To access a cell all transistors are opened apart from the considered one. As a result the operating voltage drops over the addressed cell. Finally, an additional concept, which was described by Mustafa, is the AND architecture (see figure 2.9 (c)) [70]. This is comparable with the NOR arrangement relating to the select transistor, but the plate line, which is used for the voltage inversion, is in parallel with the bit line. This creates a symmetric architecture offering an equal voltage drop over all cells and increasing the size of a row considerably in comparison with the NOR architecture. In general, all three architectures are well understood and already implemented in commercial systems. The advantage is the good controllability of each resistive switch due to its particular addressing and low crosstalk. The disadvantage is the loss of the extremely high potential of scalability as the three-terminal transistor pretends the device size and increases the complexity of the fabrication.

2.6.2 Passive ReRAM

Passive arrays for ReRAM applications surrender the use of access transistors and gain the potential of a high scalability with low cost fabrication techniques. In general, a passive crossbar array is a parallel arrangement of MIM stacks that share one electrode with the elements in its row and another one with the elements in its column. As each element is positioned at an intersecting junction, it can be addressed by its corresponding top and bottom electrode. Due to the fact that the whole device is passive, active modules for the addressing, the programming and the reading are needed. In mid-term, these logic circuits can only be implemented by active CMOS modules creating a hybrid of alternative memory and conventional CMOS technology as illustrated in figure 2.10.

The challenge of passive crossbar arrays is the accessibility of a specific junction. Parasitic

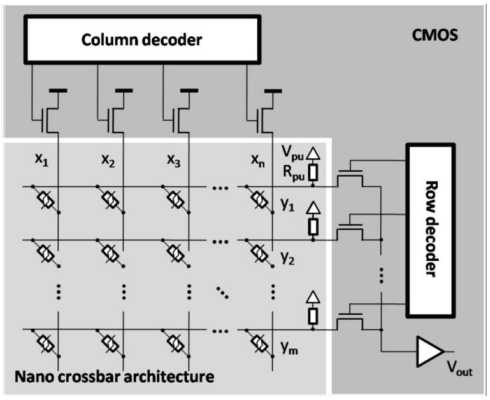


Figure 2.10: Hybrid of a nano crossbar array with external CMOS decoders for the junction access concerning reading and writing.

bypasses include the risk of crosstalk, which means that nearby junctions are unintentionally programmed or interfere with the stored information of a specific cell during its operation.

Fundamentally, a device is switched when the applied voltage exceeds the write or the erase voltage. To program a cell its row is set to V_{DD} and its column is set to *GND* (ground) or vice versa. To ensure that no other junction is charged with V_{DD}, the other row and column electrodes are charged with $V_{DD}/2$. Apart from the addressed cell the voltage drop over all junctions is correspondingly between 0 and $V_{DD}/2$.

A second writing scheme can be used if the deviations of the threshold voltages are larger than $V_{DD}/2$. In this case the desired cell is charged with V_{DD} on top or bottom and *GND* on the respective opposite electrode. The remaining top or bottom electrodes are charged with $2V_{DD}/3$ whereas the respective other electrodes are charged with $V_{DD}/3$. Advantageously, the maximum voltage drop along adjacent junctions amounts to $V_{DD}/3$. The disadvantage is however the provision of an additional voltage level.

In context of the programming voltages, the array size is also limited, because the interconnect resistance between the driver and the junction increases from the edge of the array to the center position. So, the voltage drop over the metal line increases and the voltage drop at the inner cell degrades to a value where the operation results in a malfunction of the device.

Reading is performed theoretically by the application of a read voltage V_{READ} at one row, whereas all other rows are floating and columns are grounded. The columns are linked with current-to-voltage converters that provide a corresponding signal level for LRS or HRS junctions. Comparators can interpret the stored information as ‘1’ or ‘0’ by a predefined reference level. However, the real case is essentially more complex. The resistance of the metal line as well as the signal drivers, sensing elements and the access transistors and mainly the pattern of the stored information influences the array characteristic. The result is a voltage gradient, which covers the complete array, and a multitude of sneak circuits. The addressed information interferes with this V_{READ} distribution and also with partially more attractive bypasses. A detailed description of these elements and their impact is given by Mustafa et al. and Flocke et al. [32, 71]. Three general approaches should be mentioned in this context. To compensate the gradient of the read voltage V_{READ} within an array, distributed reference cells offer a dynamic and adapted reference level for the comparators. This extends the maximum functional size of an array. An adjusted nonlinearity of the $I(V)$ characteristic from the resistively switching junction increases the signal gain by the comparators. The reason is a reduced current response of adjacent junctions in the LRS by the parasitic V_{READ}. This effect becomes ideal in combination with a varistor-like rectifier that blocks parasitic currents for lower operating voltages.

In summary, a combination with CMOS is necessary to control the resistively switching element. This is possible in form of a select transistor and access modules or by the passive array and access modules. However, the latter case offers several technological advantages, but includes also challenges considering the operation.

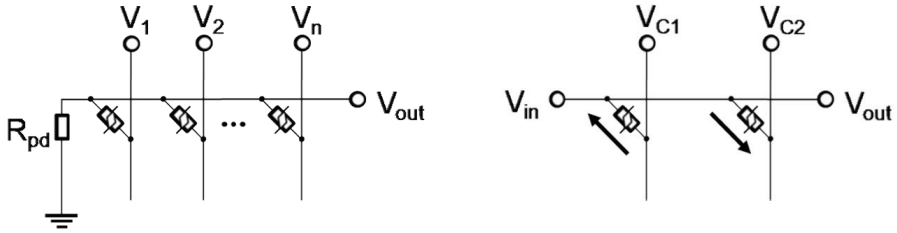
2.6.3 Logic applications

Resistive switching networks in form of nano crossbar arrays seem to be suitable for logic applications. To gain a complete set of logical functions that are necessary for computing, the following general requirements have to be fulfilled [28]: To distinguish between logical '0' and '1' a voltage swing as high as possible is necessary. A device that computes an output signal from one or several input signals needs a certain nonlinearity to provide signal levels that are distinguishable and which are essentially higher than the noise level. A second requirement is amplification. This concerns fan-in and fan-out of concatenated devices. Completely passive devices reduce the signal strength of the incoming information. From there, a chain of passive logic devices reduce the signal level down to the noise range, and a further information processing would fail. Concatenation is the third requirement, which means that output and input signals have to be compatible. This is related to the physical signal itself but also to the amplitude of the signal that defines the logical information. The need of feedback prevention, which is the fifth point, can be explained by the axiom of the directed information flow. A network of devices where everyone computes information and spreads this in all directions would lead to a loss of a defined signal level and of a sequential algorithm, of course. Finally, a complete set of Boolean operators is necessary, which includes at least an inversion (NOT) and either a disjunction (OR) or conjunction (AND) operator.

In general, resistive switching devices offer a high degree of nonlinearity, which is caused by the switching itself. In some cases, the write as well as the erase process is an abrupt jump between the LRS and HRS and vice versa. Depending on the material system, a resistance ratio of several orders of magnitude can be achieved resulting in a corresponding voltage swing. Additionally, the nature of each resistance state can comprise a nonlinear voltage or current dependency, which applies particularly for the anion migration mechanism in transition metal oxides.

Resistively switching devices, which are considered in this study, are passive devices. A network of a one-dimensional concatenation reduces the signal level depending on the occurring resistances and used fan-out. The reason is the arrangement of different voltage dividers that imply a consequent dissipation of energy. However, due to the nonlinearity, it is possible to use small networks without any internal amplification.

Finally, a simple resistor network is able to implement the Boolean functions of an AND or an OR. This is simply done by appropriate voltage dividers, which could also have been used for the resistor transistor logic (RTL) of the early 1960s and which are exemplified in figure 2.11 (a) [72]. Exchanging the constant resistances with switching elements extends the applications to reconfigurable networks and corresponding functions. In the shown example, a pull down resistor R_{pd} defines the output as ground as long as all input signal V_{in} are 0. These are connected to V_{out} via switching elements with a LRS « R_{pd} and a HRS » R_{pd}. Once, k input voltages at n cells in the LRS have a high level, $V_{out} \approx V_{in} \cdot k / n$. With a correspondingly predefined level, the output can be interpreted as '0' or '1', which can be used for an OR or



(a) (b)

Figure 2.11: (a) Resistor network implementing an AND by a corresponding voltage divider configuration. (b) Crossbar latch for the storage, restoration and inversion of a signal

AND depending on the threshold. However, an amplifier or restoration element is needed to reduce the loss of the output signal.

So, the problem is the demand for restoration and inversion. A combination of two junctions sharing one input/output line can create a bipolar latch [73]. The two crossing lines are used for the control signals V_{C1} and V_{C2} that operate the latch. The fundamental idea is the use of two reversely directed junctions. This means that one is set by a positive voltage drop, whereas the other one is reset and vice versa. The second idea is that the applied potentials at the control lines switch the junctions in dependence of the applied potential at the input line. This is called conditional switching in contrast to unconditional switching, like the programming of a memory device. A comparable proposal was also made by Mustafa et al. for the operation of memory arrays that avoid an unintended programming of neighboring cells [70]. First, a combination of pulses with high amplitudes opens both junctions unconditionally. A second set with reduced voltage pulses closes one junction and leaves the other one open in dependence on the level of the input signal. In a third step, one control line is charged with a restored logical ‘0’ and the other one with a ‘1’ signal. Depending on the assignment of these potentials to the corresponding junctions, the output signal represents the restored or the inverted input signal.

When these latches are combined with one switch at the input and one at the output, feedback prevention is given. In the beginning of the latching cycle, the input is closed and the output is open. Once the latch is programmed, the state of the switches of input and output are exchanged. Finally, the control lines are charged and the output signal is available for further computation.

In case of impedance logic, where the state corresponds to a high or low impedance of the latch and not on the output voltage, a single latch junction is sufficient as described by Snider [74].

The final challenge is concatenation, which is in this context not only related to the physical signal but also to the dimensional difference between nano crossbar arrays and sub-micrometer CMOS modules. In the previous section a complete set of logic was introduced. Nevertheless, short and mid-term solutions suggest a hybrid with conventional CMOS technology. A communication signal between a binary CMOS circuitry and nano crossbar architecture, like the mentioned memory array, needs to be adapted. In detail, the CMOS has to generate a bipolar voltage, each with at least two levels (V_{DD}/2 scheme). Also the operating voltage V_{DD} belongs

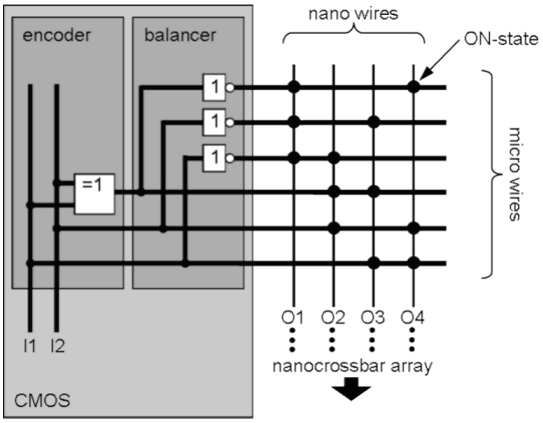
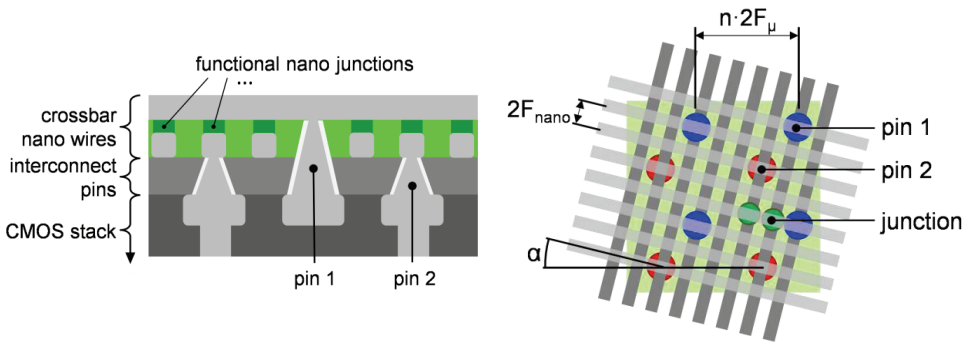


Figure 2.12: Array decoder for the addressing of junctions within a nano crossbar array [75]. The decoder is a crossbar array combining micro- and nano-lines. The microelectrodes are coupled with conventional CMOS control circuits, whereas the nano wires lead into the nano crossbar array. The decoder is uniquely programmed with the address pattern.

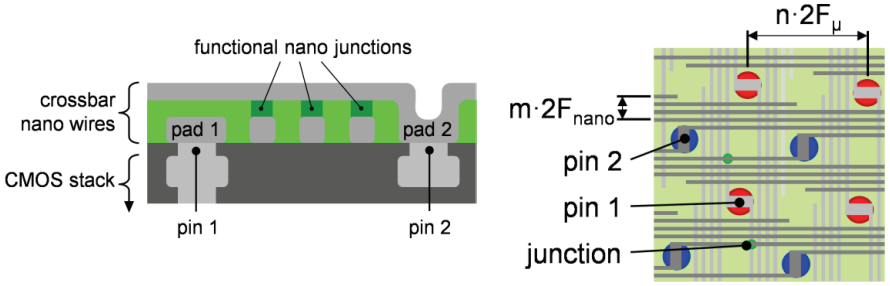
rather to the demands of the switching material than common CMOS levels. The output of a crossbar memory or logic is also rather comparable with an analog signal than a binary signal demanding for a conversion module that provides a logical signal. Both tasks are not challenging in general, but they increase the complexity of a hybrid, which might reduce the area benefit.

The second concatenation issue is related to the coupling and alignment of a real nano system and a sub-micro system. A direct alignment is not possible as the conventional resolution is determined and limited by sub-micro technology. The approach is a casual alignment, because the non-programmed crossbar array includes no locally predefined functions, and the structure is equal over the complete device. Therefore an array can be roughly aligned with a CMOS structure and subsequently be programmed. Three different techniques for a physical coupling are mentioned in the following. The simplest approach is the use of a micro/nano crossbar array where the nano wires intersect the micro wires [75]. A simple 1-hot code (the order of the input line is equal to the order of the output lines) can be used to address the junctions for the coupling. This code is written into the array comparable to the programming of a



(a) (b)

Figure 2.13: CMOL structure for a storage and logic application [76]. (a) Schematic of the via concept for the interconnection between the nano array and the CMOS layer. (b) Self alignment and addressing of a nano junction with CMOS cells by a rotation of α.



(a) (b)

Figure 2.14: FPNI structure for logic and storage applications [77]. (a) Cross-sectional view showing the via concept that provides contact pads ending on the surface level. The functional film has to be structured to connect the top electrode with the contact pad. (b) The nano wires are tilted relatively to the CMOS structures to allow for a distinct addressing.

crossbar array memory. Also more complex multiplexers, as shown in figure 2.12, are suggested in a wide range of considerations for error tolerance and redundancy [78-83].

Two further concepts combine conventional CMOS technology and nano crossbar arrays [84]. CMOL (initially a hybrid of CMOS and molecular) offers a unique connection between a CMOS circuit and a nano wire and therewith a direct addressing of a nano crosspoint junction in an array. An arbitrary CMOS control structure, which includes all interconnect levels, serves as substrate. Furthermore, vias come up from the CMOS level and end in pins with two different heights for the bottom and top electrode of a nano array, respectively. As illustrated in figure 2.13, these pins cover the surface with an equal distance. The nano array is applied with a slightly tilted angle α, which ensures that each nano wire is connected by a pin. An alignment along the pins is not necessary. Higher pins are covered with an insulating shell and disconnect bottom electrodes automatically to limit the size of an addressed set of junctions. The fabrication of the CMOL structure is however complex as the individual pins have different heights. This results in additional fabrication steps for the nano array including polishing, etching and passivation. For this reason, Snider and Williams introduced the FPNI (Field-Programmable Nano wire Interconnect) concept [77]. Different from the CMOL, the vias of the FPNI-CMOS level are flush with the substrate surface for the nano crossbar array as illustrated in figure 2.14. The diameter of these vias is large enough for a conventional alignment. The nano wires are connected at one end with a large contact pad that can be orientated over the corresponding via. Due to a shifted and tilted configuration of the wires to each other, a comparably dense set of electrodes arises despite the huge contact pads. Within this structure, the area for the top electrode vias is reduced and a covering functional thin film can be etched away conventionally. Finally, the top electrode is applied orthogonally to the bottom electrode. The metal structure follows the elevation profile of the surface, and no extra post treatment comparable with the pin of the CMOL is necessary.

3 Sample preparation

The following chapter describes the fabrication processes for different structures that are related to crosspoint junction devices and which establish the basis for passive crossbar arrays. In regard to the effect of resistance switching, MIM cells consist of the functional material, which is sandwiched between two metal electrodes. Basic structures with comparable large-area top electrodes were already extensively investigated in combination with a flat functional thin film covering a completely metalized substrate [85]. TiO_2 was one of several materials that were examined showing good results and the potential for a higher integration density.

Four general questions arose thus in regard of the resistively switching TiO_2. The first considered its potential for down scaling the cell dimensions to several ten nanometers. It was unclear if the switching of an intentionally addressed small area was reproducible throughout the whole functional thin film or whether the effect was related to special defects whose number and position present a constraint for small devices. The second question challenged the effect of the step coverage of the functional thin film. A bottom electrode on a flat substrate surface creates two highly tapered side walls. These have to be covered by the switching material. So far, it was unclear in which way parasitic effects caused by inhomogeneities in the material, its thickness and the electric field distribution might influence the resistance switching.

The third question deals with the probability of crosstalk between adjacent junctions. This is directly related to the used material system and the fabricated dimensions. Since the origin of resistance switching is still unclear; it is unknown, which area is active in the switching process even if the electrodes are small? Additionally, several publications describe arrays with less than 50 nm electrode distance, but examinations of crosstalk effects were not performed and its implications are still unknown. Therefore, it might be possible that the required volume for the switching in two neighboring junctions overlap and interferes.

Finally, the question about the feasibility of a template structure arose, because this should offer an opportunity of serious examinations of these passive but complex devices with several different materials. Until now, a large number of investigations dealt with passive arrays including numerous simplifications and assumptions. But whether these theoretical considerations are relevant and complete has to be shown by a practical investigation.

Patterning with metallization lines by a lift-off process is a flexible and well reproducible method to fabricate devices in the micro and nanometer range. A resist is patterned by radiation, either by UV-light or electron beam. When the resist is developed, the metal is applied as an additive process and depends only on its deposition parameters. Unlike a subtractive etching process where an etch stop or a good time control is compulsive, the choice of the deposited material is free. However, the stripping has to be performed with reasonable care, to prevent a particle contamination of the sample surface. After the stripping, any functional material can be deposited before the formation of the top electrode, though, epitaxial material systems are excluded. The applied processes and techniques are described in the following chapter.

In a first step, single isolated crosspoint junctions were fabricated in the micrometer range. Subsequently, their sizes were reduced to the nanometer range, to prove their scaling potential. Finally, more complex structures like $1 \times n$ nano crossbar arrays were fabricated and characterized. The emerging device is a one dimensional array with one top electrode crossing n perpendicularly arranged bottom electrodes. These were also called word structures as they can store the information of a logical word, respectively double or quad word, etc. To investigate the properties of two dimensional arrays with their parasitic bypasses and to offer a template structure for future investigations, $n \times n$ structures with $n = 8$, 16, 32 and 64 were fabricated with different line widths in the nanometer range.

3.1 Optical lithography

Initial experiments for crossbar structures were conducted in the micrometer range. Optical lithography (I-line with 365 nm) is an appropriate technique to pattern samples for a lift-off process with dimensions larger than 1 µm.

A negative lithographic process satisfies the demand for lift-off metallization. The inversion of the resist, which is shown in figure 3.1, creates the negatively tapered resist edge. This is important for a defined metal deposition preventing a metallization of the sidewalls. The latter would create erected metal fragments or lead to an incomplete metal stripping. A detailed description of UV-lithography is given by the suppliers of photoresists, e.g. in [86].

The employed photoresist was the AZ 5214E, which is a reverse resist and can be used for a positive and negative process. To obtain a homogenous film, the resist was spun onto a cleaned and dried substrate with 500 rpm for 5 s and subsequently 4,000 rpm for 30 s. An at least 5 min lasting baking step on a hot plate at 90 °C extracted the solvent and water from the resist film and prevented blistering by nitrogen during the exposure. The final resist thickness amounted to 1.5 µm. Then, the sample had to cool down and to hydrate. The exposure in combination with the alignment was performed by a MA6 from Süss MicroTec. The sample was brought in vacuum contact with the mask to obtain a resolution of 1 µm, and the exposure was performed for 12 s with an intensity of approximately 35 $mW \cdot cm^{-2}$. The resist had to outgas the generated nitrogen for at least 60 s before it was reverse-baked for another 60 s on a hot plate at 120 °C. An at least 2 min lasting flood exposure step inverted the transferred pattern. Finally, it

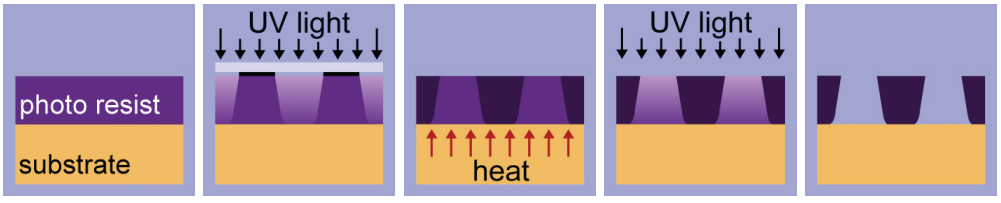


Figure 3.1: (a) Sample with applied photo resist. (b) First UV exposure transferring the mask pattern into the resist. (c) Hardening of the exposed resist volume by an inverse bake. (d) Exposure of the whole sample to break the remaining polymer. (e) Development of the inverted resist.

was developed with AZ 326 developer for 50 s in case of small patterns or longer for less critical large patterns. In summary, optical lithography is a fast and reproducible method to pattern resist films for a lift-off process. Metal line widths could be created down to 1 µm.

3.2 Electron beam lithography

Due to resolution limits, the conventional optical lithography, which is adopted in the laboratory environment, cannot be used to fabricate structures in the range from several hundred nanometers down to a few nanometers. Electron beam lithography offers a very high resolution and an adequate throughput for prototypes. An additional advantage of this tool is its high flexibility, as each pattern can be easily defined and redesigned by CAD-tools and is subsequently converted into machine compatible commands. Finally, the structure is directly written into a suitable resist. The following section gives a brief description of the machine, summarizes the physical effects that determine the writing process and explains this finally.

3.2.1 The electron beam direct writing system

The used system was a Leica EBPG 5000 from Vistec Electron Beam GmbH. The individual modules that characterize this machine are illustrated in Figure 3.2 for a better survey. This construction is of course positioned in a chamber with a vacuum cascade between 10^{-10} mbar at the beam source down to $5 \cdot 10^{-7}$ mbar in the sample chamber.

The reason for the usage of an electron beam is given by the minimum pattern size that can be transferred by its radiation and which is defined by the resolution limit l_m

$$l_m = k \frac{\lambda}{NA}. \tag{3.1}$$

k is a process and system dependent factor, which is typically between 0.5 and 0.7. The numerical aperture is given by $NA = n \cdot \sin(\alpha)$ with the refractivity n and the aperture angle α. The decisive parameter is the wavelength λ, which for example amounts to 365 nm for the i-line in an optical lithography tool. The reduction of this value is the aim of the electron beam lithography. Due to the dualism of particles and waves an electron has the wavelength

$$\lambda_e = \frac{h}{m_e \cdot v_e}. \tag{3.2}$$

h is the Planck constant and m_e the mass of an electron whereas v_e denotes its velocity. The product of $m_e \cdot v_e$ is determined by the acceleration voltage V_{acc}

$$e_0 V_{acc} = \frac{1}{2} m_e v_e^2 \Leftrightarrow m_e v_e = \sqrt{2 m_e e_0 V_{acc}}. \tag{3.3}$$

The combination of equation (3.2) and (3.3) is

$$\lambda_e = \sqrt{\frac{h^2}{2 m_e e_0 V_{acc}}}, \tag{3.4}$$

which is a good approximation to the relativistic case and valid for acceleration voltages below

100 kV. With 50 kV acceleration voltage an electron beam systems creates a theoretical wavelength of 5.487 pm. This is a gain of more than 66,500 in comparison to the UV-source. In the following it will be shown that different other effects limit the real resolution of the electron beam.

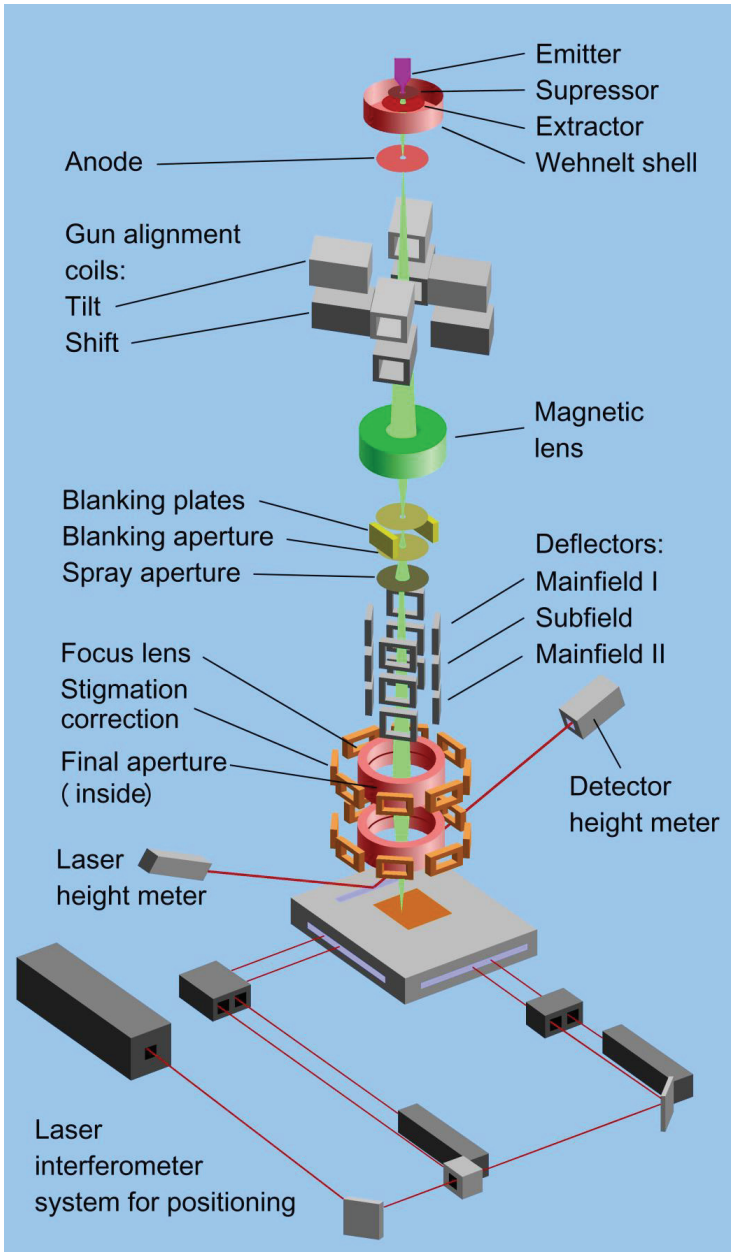


Figure 3.2: Schematic diagram of an electron beam writing system

To generate an electron beam, the EBPG system uses a combination of a thermal and a field-effect source, a so called thermal field emitter cathode. Here, a cathode of a tungsten single crystal is covered with ZrO_2 to reduce the work function. The tip is heated up to support a Schottky-emission with an applied electrical field. Due to the heat, the surface contamination is reduced drastically. The work of emission is about 2.8 eV and the emitted electrons posses an energetic distribution ΔE_e between 0.5 and 1 eV at a temperature of 1800 °C. The small energetic distribution reduces the color aberration $e_C \sim \Delta E_e$ that is caused by the dispersion of the electron energy during the deflection in the electromagnetic lenses. These values are a good compromise for a high current radiance of $5 \cdot 10^8$ A·cm^{-2}·sr^{-1} and small virtual source of about 10 to 20 nm that determines the resolution of the system.

The initially less directed beam from the filament is shadowed in backward direction by the suppressor. This is supported with a negative potential that suppresses any backward emission behind the tip. An additional extractor anode exhausts the electrons, which are created at the tip shank, and the remaining beam fraction is focused by the Wehnelt cylinder.

The negative potential of this half-shell electrode in combination with the subsequent anode generates the electron acceleration and creates a thin and focused beam. This set of electrodes presents the first electrostatic lens. Any kind of tilt and shift of the beam is compensated by a set of gun alignment coils, which can deflect the electrons electromagnetically and bring the beam back into the desired position.

The second magnetic lens focuses the beam into the blanker and works as a zoom in combination with the first electrostatic lens. Therefore, it can be adjusted between a long and a short focal distance by the exciting current in its coils, resulting in a larger or smaller beam diameter. The blanker itself is a combination of electrodes, which generate an electric field. This is used to deflect the beam completely or to blank it by its aperture, respectively, when the beam has to be in its off state. The subsequent second aperture confines the beam expansion before it enters the deflector cascade with the upper and lower main deflector and the trapezium deflector. The application of these parts is described in more detail below. The aperture is used to limit the aperture angle. This decreases the focus error caused by spherical aberration $e_{SA} \sim \alpha$. The reason is the higher deviation in the outer beam region by the electromagnetic lenses.

Finally, the beam passes a set of focus lenses, consisting of a coarse and several fine lenses that create the high resolution in the focus plane where the sample surface is positioned. These lenses are surrounded by coils, which adjust the astigmatism. In this case, the cross section of the beam becomes elliptic by unsymmetrical fields in the lenses or by particles contaminating the electro optical system. Then, the focal point would split into two planes, one where the beam fraction in x direction is in focus and a different one where the y direction is in focus. The distance between these planes Δf defines the astigmatism error $e_A \sim \Delta f$.

The values e_A, e_{AS} and e_C are combined to the total lens error, which is given by $e_{total} = \sqrt{e_A^2 + e_{AS}^2 + e_C^2}$ and which defines also the minimum resolution.

An automatically movable stage extends the accessible area and the size of the writeable substrate to six inches. The combination of beam deflection and stage movement is a challenge with regard to the necessary precision. This is gained by two laser interferometers that control the actual position of the table in x and y direction. The measurement resolution amounts to 0.6 nm what exceeds the precision of the actuator but serves additionally as feedback for the beam deflection. This can compensate the inaccuracy of the mechanical part by an offset in the deflection coils.

The height of the stage and the substrate is checked by a reflected laser beam that light onto a dual diode detector. Also here a mechanical correction is assisted by a faster and more precise focus adjustment by the corresponding lenses. If the height is determined by an incorrect measurement or the surface of the sample is not absolutely flat, the focus gets out of the surface plane, resulting in insufficient exposing doses or a smearing of the pattern as shown in figure 3.3.

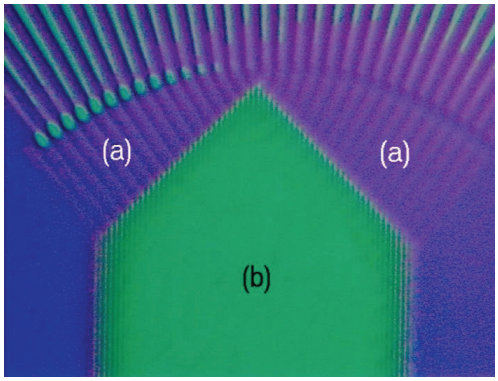
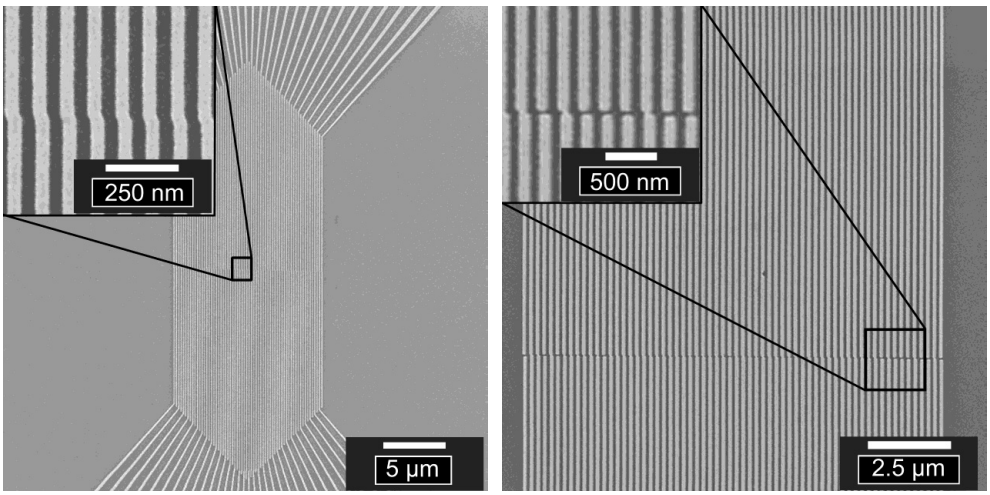


Figure 3.3: Focus out of plane due to a wrong height adjustment. As the electron dose is maximal in the focus, some structures are underexposed (a) and some are blurred when the density of the exposed areas is high (b).

Crossbar arrays and several other applications consist of several structured layers that have to be aligned to each other. This is accomplished in the nanometer range by the electron beam system. The position of the sample is determined by contrast marks, which are detected in a scanning electron microscopic mode. Three marks in the outlying corners of the pattern are required for the alignment in x-y-direction. Their predefined shape is a square with 20 µm edge length. In a lift-off process, each mark can only be used once, because its detection exposes the mark and the surrounding area. So, every layer needs its own mark. After a rough manual alignment of the sample, the system scans a default region around the predefined position. A slight distortion of the bottom structure is automatically corrected compensating tolerances of the previous writing. So, additional marks, called infield marks, increase the accuracy of the process. The pattern is normally designed by a CAD program, which generates an ASCII-table containing the shape and position of the pattern. This can also be done manually for simpler patterns. A final conversion, done by CATS from Synopsis, transcribes the pattern to meet the demands of the writing strategy of the machine.



(a) (b)

Figure 3.4: Stitching errors at the border of a block due to a shift of two pattern sections against each other. The sections can be slightly shifted into any direction resulting in a kink (a) or a disconnection (b).

The electron beam system passes through the spacious pattern by the stage movement. Therefore, the pattern is divided into comparably large rectangular blocks. To write the complete substrate, the stage is moved from one block to another. The beam, however, can cover a maximum area, which is called main field. Due to physical limitations it is prohibited to write outside the main field. So, the blocks have to be smaller than this area to reach every part of the sample surface. Typically, most patterns are larger than a block size, therefore a block is written completely before the stage is moved and the next block is written. The border of the first block has to be exactly aligned to the border of the next block, which is called stitching. As the mechanical system is limited in its precision, very small structures can be shifted or dissected at this border as shown in figure 3.4. To prevent such an effect the nano pattern has to be positioned in the center of a block and not at the border. Larger structures are not affected by the stitching. Here, the writing parameters compensate such inhomogeneities by dark field exposure, which is explained in the following.

Each main field is divided into smaller subfields. The subfields are written one at a time similar to the blocks. But as patterns can normally cross the border of a block or a subfield, they are subdivided into trapezoids ending at least at these borders. Besides the alternating movement of the beam and the stage, the splitting of the pattern in several sections increases the performance of the machine. This means in detail that the pattern and the trapezoid generator are optimized to perform the process most effectively by guiding the beam through the actual pattern section while calculating the next section. The available address space is 32 bit large for each main field whereas each address corresponds to a pixel. The size of a pixel, called spot size, defines the resolution, which was 5 nm in most cases. As a result, the main field had a size of $327.68 \cdot 327.68\ \mu m^2$, and the chosen block size was $320 \cdot 320\ \mu m^2$. The less significant 20 bits contain the address fraction of the subfield, which corresponds to 1024×1024 pixels. Each pixel

is generated by a short exposure, whereas the distance between each spot is defined by the beam step size. To write a complete area, the spots have to be next to each other, whereas the beam step size corresponds here to the diameter of the spot.

Within each main field the beam is directed by the main deflector coils to the starting position of the writing step, which is called 'vector-scan'. This is normally the lower left edge of a trapezoid. Then, this is scanned by the trapezium deflector coils, which guide the beam like a meander through the intended pattern, point by point to the upper right corner. During this scan the beam stops at each point to generate the desired dose by the exposure time. The beam is blanked once the trapezium is written and guided to the next starting point where it is unblanked again.

The real spot has a Gaussian intensity distribution, which can be described by the current density due to the electron flow,

$$J(r) = J_0 \cdot e^{-\left(\frac{r}{\rho_{Spot}}\right)^2} . \tag{3.5}$$

The beam shape is defined by the spot size corresponding to the diameter d_{Spot}, or its radius ρ_{Spot}, respectively, There the current density amounts to $J_0 \cdot e^{-1}$, with its maximum J_0. A 2-dimensional illustration of this distribution is presented in figure 3.5. The second parameter is the beam current, $I_{Beam} = \iint_F J(r)dA$, that adjusts the dose in combination with the stepping frequency f_{Step}, which is the third parameter for the writing process. The average dose D is then given as

$$D = \frac{I_{Beam} \cdot}{\pi \cdot \rho_{Spot} \cdot f_{Step}} . \tag{3.6}$$

A significant effect concerning the resolution is the proximity effect. It is caused by the interaction of the incident electrons with the present matter. In this case, this is the double layer resist and the substrate consisting of Si and SiO_2 and eventually TiO_2 and a combination of Ti

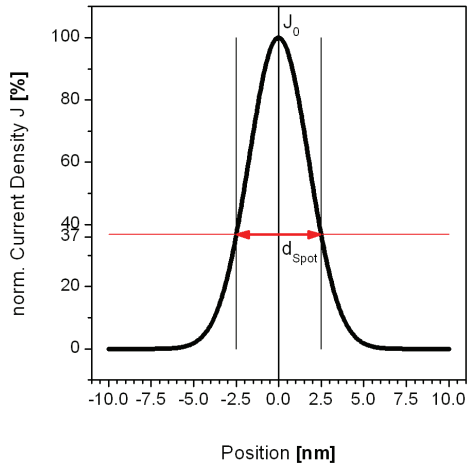
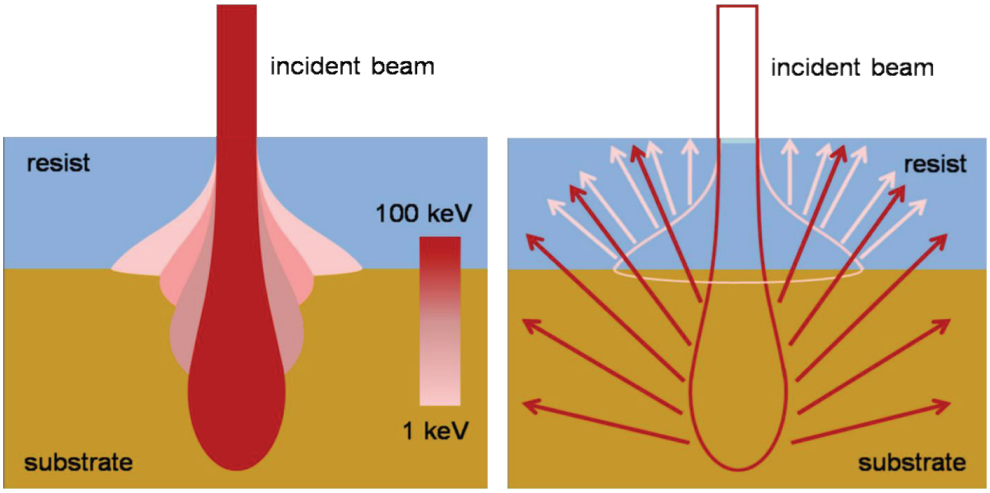


Figure 3.5: Distribution of the current density of a Gaussian beam.



(a) (b)

Figure 3.6: (a) Schematic illustration of the distribution caused by the forward scattering of an incident beam. (b) The corresponding illustration for the backscattered electrons.

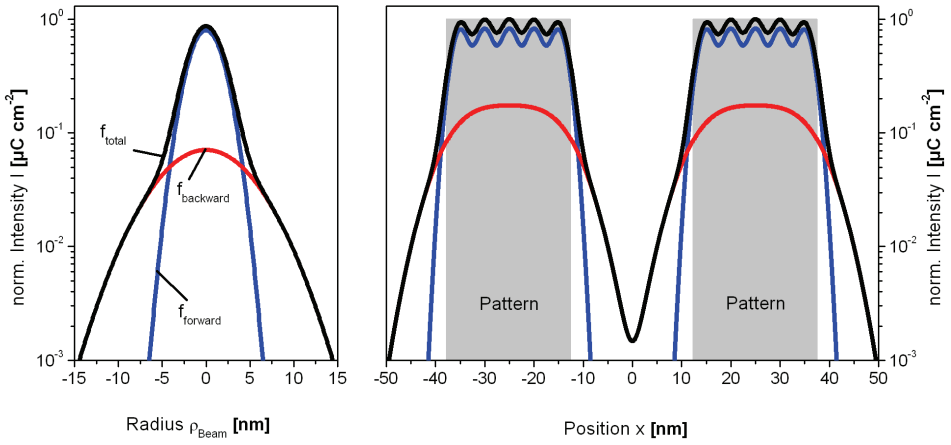
with Pt in the case that bottom electrodes were already deposited. The trespassing electrons are scattered elastically at the inertial mass of the positively charged nucleus, which results in a deflection from their original path. As a consequence, the originally well focused beam expands the deeper it gets into the matter. Due to a high penetration, scattering still occurs deep in the substrate and the fraction of returning electrons pass and expose the resist besides the incident beam. Additionally, the primary electrons interact inelastically with the electron shells of the matter and generate secondary electrons.

The distribution of the incident beam has a Gaussian nature as already mentioned. This is retained by the scattering, but the corresponding standard deviation increases and splits up into forward and a backward fraction, named β_{FWD} and β_{BWD}, respectively, corresponding to the forward and the backward scattering. Figure 3.6 illustrates the fractions schematically. With the ratio between the forward and the backward fraction η the dose distribution within the resist, depending on the radius around the beam center, is given by

$$f_{total}(r) = f_{forward}(r) + f_{backward}(r) = \frac{1}{\pi(1+\eta)}\left[\frac{1}{\beta_{FWD}^2} e^{-\frac{r^2}{\beta_{FWD}^2}} + \frac{\eta}{\beta_{BWD}^2} e^{-\frac{r^2}{\beta_{BWD}^2}}\right]. \tag{3.7}$$

The result is an expansion of the exposed area leading to a dispersion of the dose distribution. The acceleration voltage can be used to control the proximity effect as the forward scattering decreases with an increase of the kinetic energy of the electrons, illustrated in figure 3.6 (a). For example, the penetration depth is a meaningful value in this context. It amounts to 30 µm in Si for an acceleration voltage of 50 kV and is still above 1 µm for 10 kV.

So, all electrons pass the complete stack nearly unscattered due to the use of very thin films in the sample setup. Also the insulating SiO_2 layer is passed, and the Si discharges the penetrating



(a) (b)

Figure 3.7: (a) Distribution of the forward (blue curve) and backward (red curve) scattered electrons of an incident beam with a Gaussian distribution. The black curve presents the total distribution. (b) Superposition of all fractions for a pattern with two structures. The intended pattern is illustrated by the grey fields.

electrons. Additionally, high acceleration voltages create a better resolution of the incident beam. So, the extension of the intensity distribution for the forward scattering can be neglected. In contrast, the backward scattering increases with the acceleration voltage and, with that, its influence on proximity. Due to a wider distribution of the backscattered electrons, as illustrated schematically in figure 3.6 (b), the fraction compared to forward scattered electrons is generally low. So, the intensity is essentially smaller and a single spot or a small structure does not widen significantly as shown in figure 3.7 (a). However, if the intended pattern occupies a larger fraction of the total area, the superposition of the backward fraction creates a significant background exposure, even in the unwritten regions. This is the case when several adjacent structures of a pattern get very close to each other, which is typical for a large set of parallel metallization lines in a crossbar array. Figure 3.7 (b) exhibits the background exposure between two patterns, possibly exceeding the contrast value of the resist. The expanded fractions of the backscattered electrons overlap between the intended regions and also expose the gap of the structure. In the following, it becomes obvious that the proximity is a challenging effect for the fabrication of crossbar arrays, as these are exemplary for a dense pattern with small structures. The task is the adjustment of the dose depending on the acceleration voltage into a range where the contrast between exposed and unexposed regions meets the demands of the resist. However, an advantage of the proximity is a balancing of process inhomogeneities like stitching.

3.2.2 Resist chemistry of the PMMA and the PMMA/MAA

PMMA (polymethyl methacrylate) is a proven positive resist and extensively used for electron beam direct writing. The combination with PMMA/MAA (methacrylic acid) offers several advantages for lift-off processes. Most important is the negatively tapered resist edge that is shown in figure 3.8.

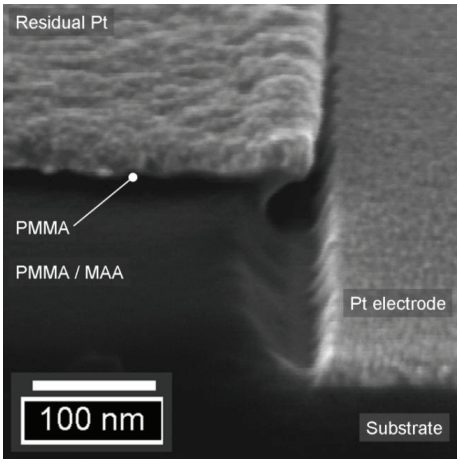


Figure 3.8: Cross sectional view on a two layer resist at a breaking edge.

PMMA originates from the polymerization of the monomer methyl methacrylate (MMA) to long molecular chains. The length of these molecules is described by the molecular weight M_0 with the unit $g \cdot mol^{-1}$, which is simply abbreviated by the weight in 'k', standing for $kg \cdot mol^{-1}$. The molecular weight is defined by

$$M_0 = \frac{m * N_A}{N_0} \tag{3.8}$$

with the mass of a sample volume m, the Avogadro's number N_A and the number of molecules in the sample volume N_0. Commercially available resists have a molecular weight between 50k (50,000 $g \cdot mol^{-1}$) and 1500k (1,500,000 $g \cdot mol^{-1}$). The fundamental functionality is the controlled local exposure of the molecules with an electron beam. In the considered case, the energy of the accelerated electrons is larger than the potential of the molecular bonding and splits these chains in shorter sections. Emerging decomposition products are dissolved and removed during the development. Because long cross linked chains are essentially more stable, the developer removes the short chains faster, which results in a positive transfer of the written pattern into the resist.

An important parameter is the sensitivity, which can be described as the dose of charge per area that is necessary to obtain a complete exposure of the resist. This can be interpreted by the intensity of the resist reaction, here the splitting of molecular chains, caused by the electron dose. However, the abrasion rate during the development depends on the absolute weight of the molecules, which also means that a resist with a low molecular mass is diluted faster. Therefore, these resists show an essentially higher sensitivity as their weight is already reduced in the unexposed state and the removal of unexposed or less exposed material is higher. Additionally the dark field exposure consigns a higher impact.

On the other hand, the probability for chain scissoring is much higher for a high molecular weight. For this reason the number of divided molecules is essentially larger and their molecular mass is reduced stronger. An adapted high dose results in a higher contrast between the exposed and the unexposed material. The contrast is a composition of the contrast created by the partial

exposure and the contrast generated by the development of the resist. For a positive tone process it is defined as

$$\gamma_{pos} = \frac{1}{\log\left(\frac{D_1}{D_0}\right)} \tag{3.9}$$

with the electron dose D_0 where the resist remains insoluble and D_1 where the resist becomes completely soluble.

These are important properties for the combination of layers with a low and a high molecular weight. The former provides a high sensitivity that results in overdeveloped structures by common doses, whereas the latter provides a high contrast and maps the defined patterns well. This means in detail that the higher sensitivity of the copolymer creates a larger expansion of the resist gap during the development. For this reason, the copolymer PMMA/MAA is the bottom and the PMMA is the top layer, which generates in this combination a staged overhanging upper resist edge as shown in figure 3.8. In doing so, the created gaps contain no resist residues and no fencing occurs. Additionally, the stripping for the lift-off can be performed easily as the solvents have enough space to launch into the resist.

3.2.3 Lift-Off patterning

The following section describes the process flow for the patterning of nanometer crossbar arrays in detail. The used standard substrate was a 1” · 1” Si wafer with a thermally oxidized surface to create a several hundred nanometer thin insulating layer. The applied resist was composed of two different layers that satisfied the above mentioned demands concerning contrast and sensitivity. The lower one was the PMMA/MAA, named AR-P610.01, distributed by Allresist. It was applied via spin coating by a 5 s lasting casting step with 500 rpm and a subsequent thinning step for 30 s with 1000 rpm creating a homogenous distribution of the resist thickness. The resulting layer thicknesses are given in table 3.1.

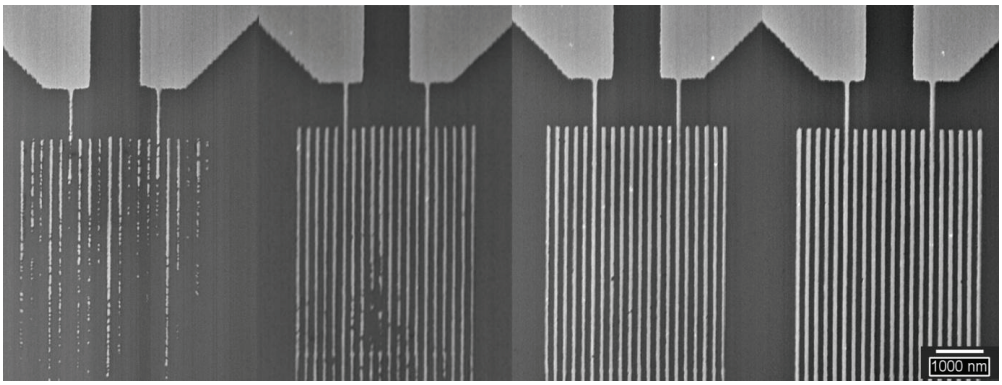
Table 3.1: Resist thickness depending on the layer sequence

No.	Resist	Number of Layers	Thickness [nm]	Theoretical thickness [nm]	Difference [nm]	Loss per application [nm]
1	**PMMA/MAA**	**1**	**39**	**39**	**0**	**0**
2	PMMA/MAA	2	59	78	19	19
3	PMMA/MAA	3	76	117	41	20.5
5	**PMMA**	**1**	**48**	**48**	**0**	**0**
6	**PMMA/MAA PMMA**	**1+1**	**75**	**87**	**13**	**13**
7	PMMA/MAA PMMA	2+1	95	126	31	18.5 + 12.5

Finally, the film was dried and stabilized for not less than 2 min on a hot plate at 210 °C. To obtain thicker resist layers it is possible to repeat this step several times before applying the top layer. This is a PMMA, named AR-P 671.01 with a molecular weight of 950k. The second layer was deposited by a casting with 500 rpm for 5 s and a subsequent 30 s lasting spinning at 6000 rpm. It is also dried for 2 min on a hot plate but with a reduced temperature of 180 °C. Afterwards it can be directly used for the electron beam direct writing. The thickness of the resist was determined by profilometry over a prepared resist edge. To describe the mutual influence of multiple subsequently applied layers and to estimate the potential for thickness modifications, also the combination of different layer stacks was tested. As shown in table 3.1 a single PMMA/MAA layer had an average thickness of about 39 nm. Every additional layer increases the thickness for about 19 nm. This reduced gain of film thickness was caused by a new dissolution of the lower layer during the application of a new coating. A single PMMA layer had an average thickness of 48 nm, whereas the combination with a PMMA/MAA reduces the total thickness by about 13 nm. In the following, it is shown that the proximity effect narrows the bar of the copolymer distinctly. From there, only a single layer was adopted to prevent a bending or a rupture of the material. This was adequate as the thickness of the metal should not exceed 30 nm to minimize the step height for all consecutive layers.

Effective beam spot sizes of 100 nm and 5 nm were used distinguishing between structures larger and smaller than 1 µm. This increased the throughput drastically as most structures belong to the large supply lines.

To determine an appropriate dose several series were performed. In this context a structure was repeatedly written with increasing doses from 100 $\mu C \cdot cm^{-2}$ to 300 $\mu C \cdot cm^{-2}$. As the pure insulating resist cannot be examined by an SEM, the intended metal was deposited before the subsequent inspection. Figure 3.9 shows the results of such a dose test: below 140 $\mu C \cdot cm^{-2}$ only sporadically distributed metal dots were observed on the sample surface. Higher doses

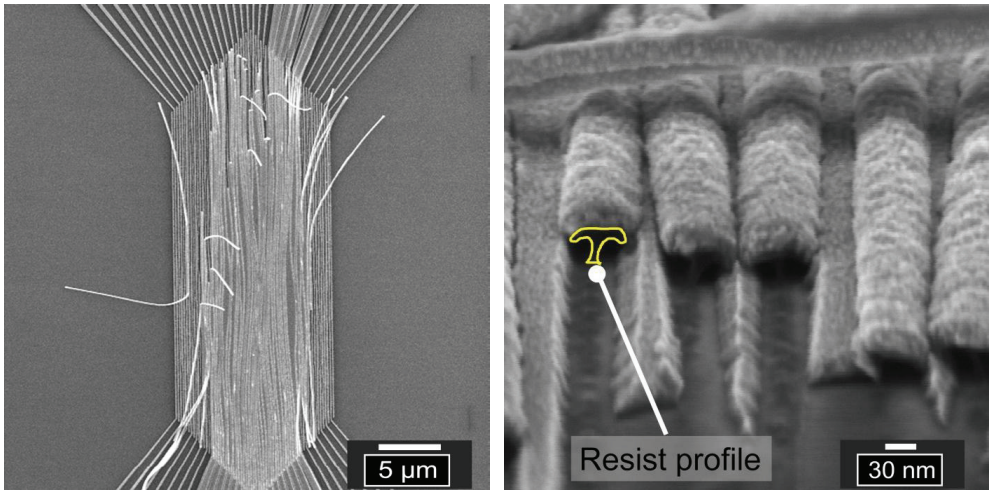


(a) (b) (c) (d)

Figure 3.9: Scanning electron micrograph of a dose test series with 140 (a), 160 (b), 180 (c), and 200 $\mu C \cdot cm^{-2}$ (d). The examined structure consists of 20 parallel lines with 100 nm line pitch and 100 nm distance.

generated a more and more complete structure until the wires were continuous at around 180 µC · cm^{-2}. The aimed ratio between wire width and distance was finally reached at a dose of 200 µC · cm^{-2}.

Also single devices could be generated with this dose, even though their width was somewhat lower. Here, doses up to 400 µC · cm^{-2} expanded the resist gap and finally the electrodes. This becomes necessary for structure sizes below 100 nm down to 40 nm. The picture also exhibits the proximity effect, as the structures near the huge supply electrodes in the upper part are better developed. However, resist structures became instable above 240 µC · cm^{-2}, which becomes apparent in figure 3.10. Here, the copolymer in the center of the structure is completely developed. The PMMA is directly connected with the substrate and the lift-off fails due to the lack of the overlap of the resist edge. Some PMMA bars were additionally floated away during the development. The cross sectional view reveals the reason by showing the thin bars of the lower resist that offer only a low stability for the process. From there, all structures were fabricated with a dose of 200 µC · cm^{-2} and a beam current of 104 nA for the coarse and 1.049 nA for the fine layer, yielding a writing frequency of 5.221 MHz and 20.9740 MHz (note equation 3.6). The development was performed in AR 600-56 from Allresist for 70 to 75 s, and then stopped in isopropyl alcohol for 1 min.



(a) (b)

Figure 3.10: (a) Fragmentary lift-off due to overexposure with a dose of 240 µC · cm^{-2} for a 64 bit bottom electrode with 100 nm line width. (b) Cross section of a 50 nm wide structure with broken and shifted resist structures in the lower layer.

3.3 Metallization

In the context of this study, two different deposition methods for metal layers were used. The first one was DC-sputtering and the second one was electron beam assisted thermal evaporation. Both processes were tested for the fabrication of micro-lines. Pt served as electrode material because of its inert and non-diffusive properties. A thin Ti Layer was needed to promote adhesion of the Pt layer onto the SiO_2 substrate or TiO_2 film.

3.3.1 DC- sputter deposition

Sputtering belongs to the physical vapor deposition (PVD) techniques, as the thin film is deposited by condensation out of the vapor phase of the desired material. The sputtering system that was used for the layer deposition was a Univex 450C from Leybold. This sputter machine was designed as a cluster tool with a load-lock and several chambers equipped with different materials like Pt or Ti, each connected with the transfer chamber. The setup enabled a consecutive in situ deposition of different materials.

A DC-magnetron source was used for the fabrication of Pt and Ti thin films as depicted in figure 3.11. This was adequate for the pure metal targets, which were connected to the negative potential of the generator serving as cathode. The grounded substrate support established a high electrical field with the target. Pure Ar was injected into the chamber resulting in a working pressure between 5.1 and $13.5 \cdot 10^{-3}$ mbar. This pressure and the high electric field ignited an Ar^+ plasma, which is also termed glow discharge due to its relatively low ionization degree. Under the given parameters and a DC input power of 375 W, a deposition rate of 2.5 $Å \cdot s^{-1}$ for Pt was achieved. The material transport was undirected and isotropic due to the large diameter of the 4 inch target and the small distance between target and sample. This effect was strengthened by the comparably high working pressure resulting in a high collision rate of the sputtered material (meaning free path length ~mm [87]).

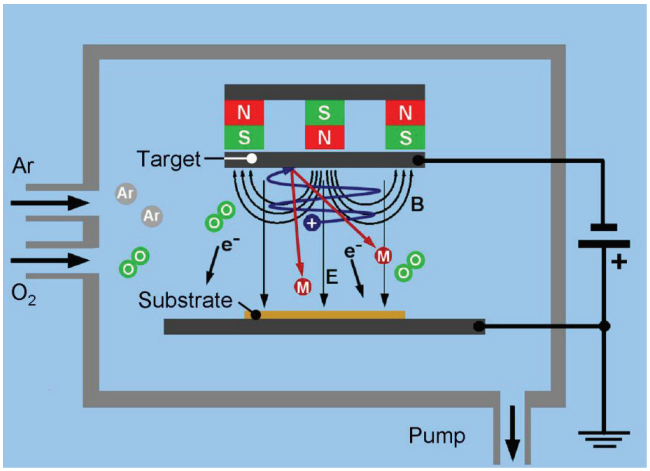
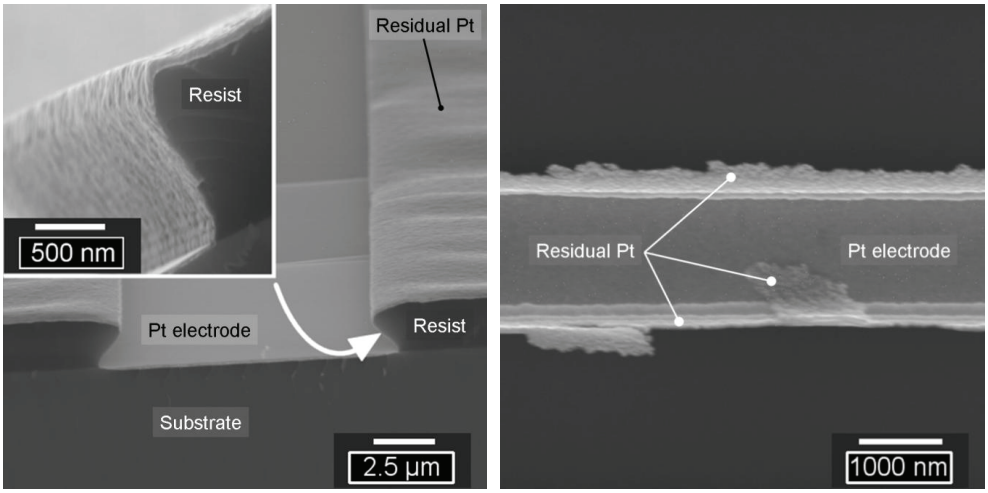


Figure 3.11: Schematic description of a DC- magnetron sputtering process. Ar can be mixed optionally with O_2 to obtain a reactive sputter process for the generation of a TiO_2 out of a Ti target.



(a) (b)

Figure 3.12: (a) Metal film sputtered onto a resist structure. The bottom of the gap as well as the resist sidewalls (see inset) are completely covered with Pt. (b) Metal electrode and residues after the resist stripping.

The distribution of collided particles along their travel distance x is $N(x) \propto e^{-\frac{x}{\lambda_p}}$, whereas their mean free path $\lambda_p \propto 1/p$, with the pressure p [88, 89]. A metal covering of the resist sidewall was the consequence even for inclined edges with a huge shadowing overhang. Figure 3.12 (a) clarifies this effect. During the following stripping of the lift-off process, it was hard to remove the resist that had been hardened by the ion penetration of the sputtering. Additionally, the metal that primarily covered the sidewalls of the resist edge stuck on the substrate and could not be removed. The occurred residues, named ears, are shown in figure 3.12 (b). Because of these resist and metal residues, sputtering of Pt was critical for a lift-off metallization.

3.3.2 Thermal evaporation

Metals such as Pt and Ti were also deposited thermally in a high vacuum (HV) chamber with a background pressure of about 10^{-7} mbar. The pure metals are stored as solid nuggets in water cooled tungsten crucibles. A directed electron beam is used to melt the metal. The corresponding gun is positioned under the evaporation source, shadowed against the metal vapor to prevent a contamination. The electrons were accelerated and directed into a circular beam course, which is guided around the crucible by a magnetic field and impacts onto the surface of the evaporation material. The evaporation rate, which was between 2 and 5 Å·s^{-1}, can be adjusted by the beam current of the gun. This value is controlled by the deposition rate monitored in situ by a quartz crystal microbalance, which serves also for the thickness control of the layer. Figure 3.13 shows the described facility to clarify this process.

This method is dedicated for lift-off metallization for the following reasons: The impacting electrons heat up the target partially, which is nearly creating a spot source. Vaporized metal

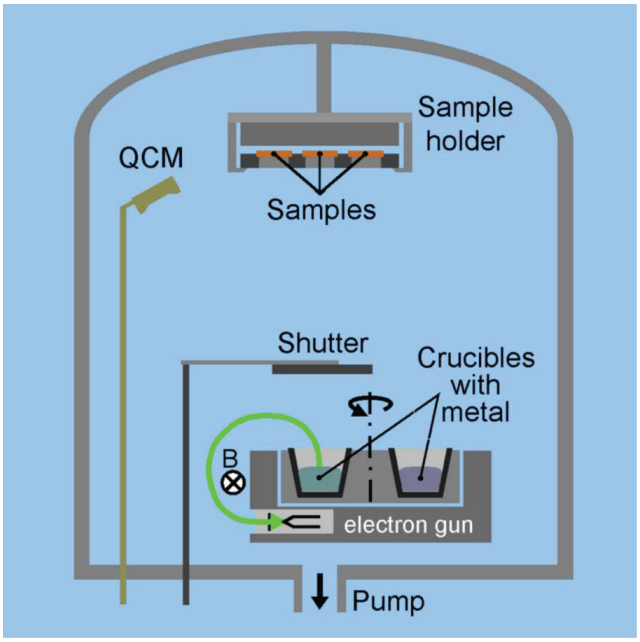


Figure 3.13: Schematic of a vacuum chamber for electron beam assisted thermal evaporation.

atoms leave this with a low kinetic energy (1/2 $k_B T$) on a straight path, caused by a long mean free path in the UHV. The samples are positioned in the upper part of the chamber, facing the material source that is about 50 cm away. In combination with the small dimensions of the pattern and the resist structure (~ µm), this results in a very anisotropic or directed deposition. Figure 3.14 clarifies the resulting feature by distinct shadowing of the metal vapor by overlapping resist edges.

The kinetic load for the sample and the resist is very low (~ 0.1 eV) due to the high distance to the source and the low energy of the metal atoms. Additionally, the thermal mass of the sample holder was extensive enough to keep the sample at room temperature. In comparison

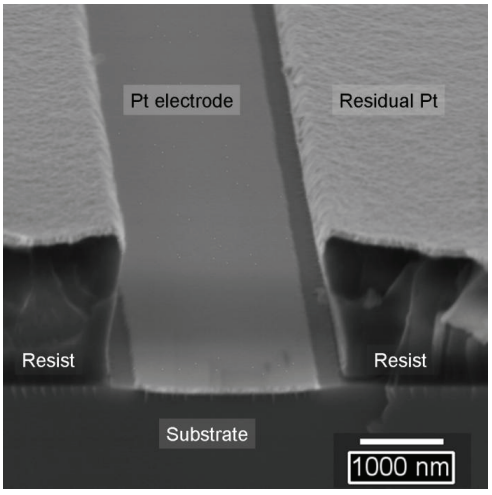


Figure 3.14: Electrode metallization by electron beam assisted evaporation.

with sputter deposition, no ion bombardment penetrates the resists and the kinetic energy of the metal particles from the vapor was one order of magnitude lower than for the sputtering [87, 90]. The result is a fast and reliable resist stripping without the formation of metallic ears. Therefore, it is altogether a suitable method for lift-off metallization.

Remarks about stripping

Finally, the spare metal on top of the resist has to be removed by resist stripping. A decomposition of the resist in acetone for several minutes with a permanent solvent flow removes the metal as far as possible. Remaining resist residues were then detached by boiling the sample gently in acetone or heating it for several hours in N-Methyl-2-pyrrolidone (NMP). Due to the energetic load during sputtering and dry etching, the stripping time has to be extended. The exact impact of the usage of an ultra sonic bath is unknown, but several structures showed defects after this kind of mechanically assisted stripping. Also the surface cleaning by applying an oxygen plasma destroyed the electrodes. The details are unknown, but the scanning electron micrographs in figure 3.15 suggested an enormous heat, which might be the result of a turbulent flow in the metallization lines due to the induction by a RF-field.

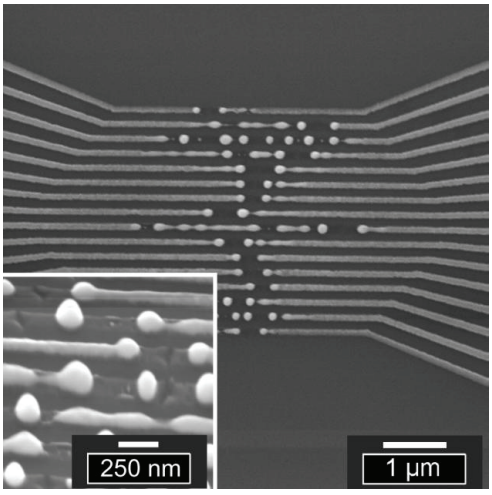


Figure 3.15: Destruction of the 100 nm bottom electrodes within the center of a crossbar array by oxygen plasma cleaning. This kind of damage depended strongly on the layout of the structure. These kind of metal drops shown in the inset infer on a high temperature.

3.4 TiO_2 deposition

Two deposition methods were used to condense the thin TiO_2 films that served as a functional layer. Atomic layer deposition (ALD) was applied based on a successful investigation of unipolar resistance switching [24]. For comparison, reactively sputtered TiO_2 was also incorporated into micro crosspoint junctions. Its high availability and successful application as material in memory devices led to its integration into nano crosspoint junctions [91]. The following section of this chapter will introduce the fabrication method for ALD and reactive sputtering and describes basically the virgin properties of the fabricated thin films.

3.4.1 Atomic layer deposition

ALD belongs to the chemical vapor deposition processes since growth of the layer is due to a chemical reaction of the gaseous precursors. The advantage of this technique is its isotropic deposition characteristic, which is applicable for large aspect ratios that occur, for example, in the narrow trenches of advanced DRAM capacitors [29]. This feature was also of use to cover the steps created by the bottom electrodes of a crossbar. The origin of the isotropic deposition is the direct and exclusive reaction of the precursor with a suitable but geometrically arbitrary surface creating a monolayer. In the ideal case, the process control of the ALD is a reaction limited instead of a diffusion limited deposition. This is assured by the periodic exchange between two or more reactants where each of them creates a single monolayer on top of the previous one and suppresses self-consistently a further reaction and growth unlike common chemical vapor deposition (CVD). The complete surface is covered unless the injection cycles for the precursors are long enough to provide a complete exchange between active molecules and volatile byproducts.

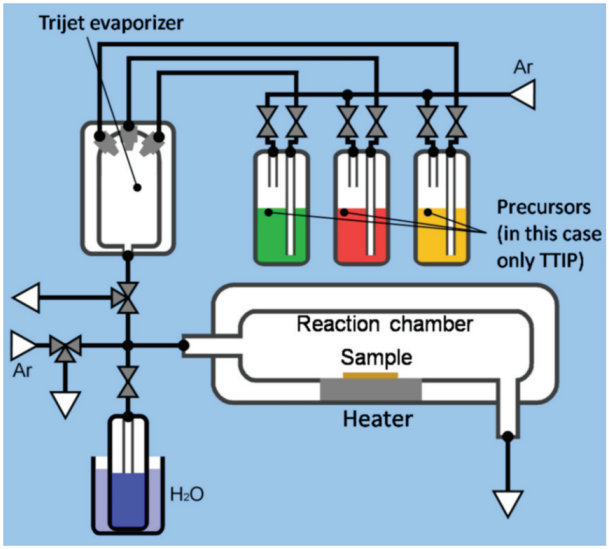


Figure 3.16: Scheme of an ALD system with several sources for precursors.

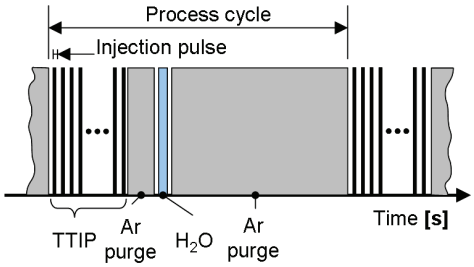


Figure 3.17: ALD process cycle with TTIP and water injection, each terminated with an Ar purge.

Additionally, a geometry dependant inhomogeneity is avoided, because the reaction stops after the first layer. A reaction between different reactants in the gas phase is suppressed by purging the chamber after each step with an inert gas. As each cycle deposits only one layer, this method offers high controllability for the film thickness and properties.

The ALD tool was an AIX200 CVD pilot system from Aixtron, which was upgraded for sequential gas injection. As Ti precursor titanium tetraisopropoxide $Ti[OCH(CH_3)_2]_4$ or TTIP was used. The precursor was dissolved with an amount of 0.05 - 0.22 Mol in ethylcyclohexane (ECH) as a buffer to obtain a better process control. In comparison with other solvents ECH contained less water, which initiates the TiO_x growth. Additionally, it did not modify the carbon compound of the precursor [92].

Figure 3.16 illustrates the setup of an ALD facility for three optional precursors. The liquid precursor solvent mixture was first injected into a tri-jet vaporizer, kept at 200 °C. The Ar carrier gas was used to purge the TTIP with 200 sccm into the reactor, which had a process temperature of 240 °C. The injection time was 2 ms, and the amount of the injected TTIP solution was controlled by the number of injections per deposition cycle as shown in figure 3.17.

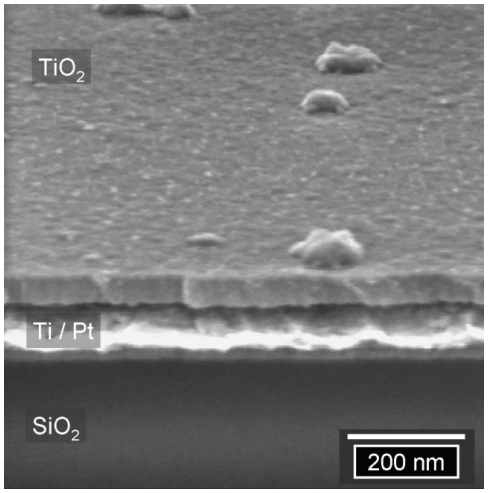


Figure 3.18: SEM cross section of a nearly 50 nm thin TiO_2 film on a Pt bottom electrode substrate.

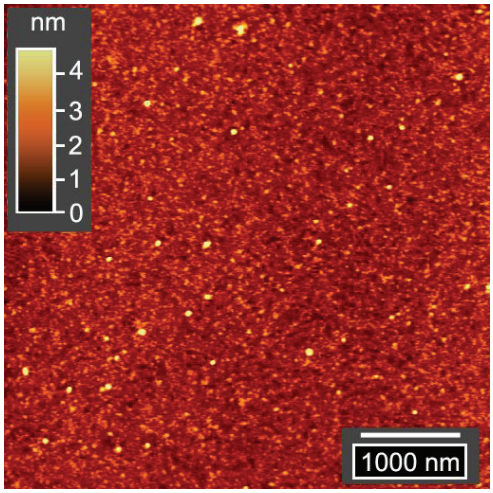


Figure 3.19: AFM scan of a 30 nm thin ALD-TiO_2 layer.

A subsequent Ar purge with 500 sccm for 3 s removed the excessive TTIP. The subsequently injected reactant was H_2O, which evaporated by its own vapor pressure at 10 °C.

To inhibit a later reaction with residual water, an Ar purge was performed for 20 s. This procedure was repeated until the desired film thickness was achieved. Unfortunately, it was not possible to setup a self-regulating deposition. It is assumed that a catalytic decomposition of the precursor in combination with the generated TiO_x surface took place. Evidently, this could not be stopped after the first monolayer, but it continued as long as reactants reached the surface. Additionally, the process created water as a byproduct that reacted again with the precursor and generated further water leading to a chain reaction. Finally, the layer growth was controlled by a high cycle frequency, which reduced the proportion of the catalytic growth and led the process to a nearly ALD type characteristic.

XPS measurements indicated 25% of residual carbon in the film, whose impact on the layer properties is unknown so far [92]. X-ray diffraction was performed to characterize the texture of the deposited TiO_x layers. θ-2θ scans as well as grazing incident examinations showed an amorphous texture without any peaks. The cross section of a 45 nm thin film on a SiO_2 substrate was used for SEM examinations. The picture shown in figure 3.18 indicates a dense film showing no directed crystal structure. The mean surface roughness was 1.7 nm with insular peaks up to 9 nm, which is confirmed by Figure 3.19, showing a rough and grainy surface.

3.4.2 Reactive sputtering

The second method that was employed to deposit resistively switching TiO_2 was reactive sputtering. This technique also belongs to the group of PVD processes, because the Ti vapor was sputtered out of a pure Ti target, and the thin film grew by condensation on the substrate surface independent of the additional oxidation reaction. In comparison with ALD or CVD, respectively, no additional chemical step proceeded concerning the adsorption of the material. The formation of TiO_2 took place by a redox reaction of the Ti vapor and the O_2 reaction gas. The latter is ionized like the process gas by the glow discharge and oxidizes the Ti on the sample. In the ideal case pure TiO_2 is formed, but it cannot be excluded that Ti rich phases condensate on the sample.

For the fabrication of TiO_2 a DC magnetron source is used as described in the upper section and in figure 3.11. In contrast to the sputtering of pure metals, a mixture of 77 % Ar and 23 % O_2 was injected into the chamber with a working pressure of $22 \cdot 10^{-3}$ mbar. The process had no additional temperature control and was assumed to be performed at room temperature or slightly elevated temperatures due to the exothermic formation of the TiO_2 and the bombardment with particles in the plasma. Figure 3.20 presents the deposition rate and the film thickness depending on the sputtering time. Thinner films were measured by X-Ray fluorescence and the standardization of the areal density by the volume density of TiO_2 [63]. For thicker layers the thicknesses were determined by cross sectional SEM pictures. Both measurements indicate a sputtering rate of $1.8\ \mathrm{nm} \cdot \mathrm{min}^{-1}$. In comparison with the ALD thin films, SEM pictures of

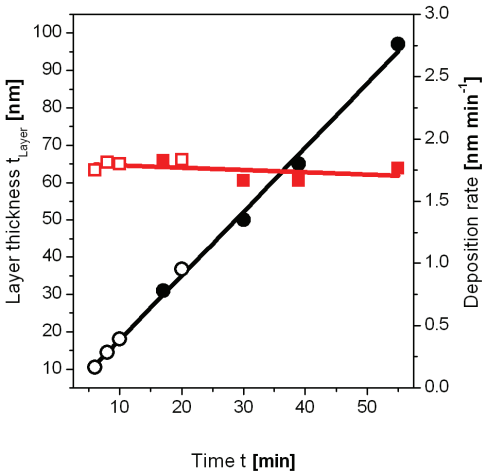


Figure 3.20: Deposited TiO_2 depending on process time for reactive sputtering. The open symbols are extracted from data of D.S. Jeong [63]. The closed symbols are results obtained by SEM measurements.

sputtered layers depicted a columnar, grainy structure, which is shown in figure 3.21. The picture also indicates a dense and homogeneous layer. Figure 3.22 displays an AFM scan of a 30 nm thin TiO_2 film on a platinized SiO_2 substrate.

The surface renders the grainy structure with an average mean square roughness of 2.4 nm and sporadic peaks with a height of 6 to 7 nm. In comparison to electrodes with thicknesses of several ten nanometers, these values were around one order of magnitude smaller. So, it was possible that the surface roughness could influence the device characteristic. However, the already mentioned chamber geometry in combination with the comparable high process pressure leads to an isotropic deposition characteristic. This satisfied probably the demand for homogeneous step coverage of the nano electrodes.

To prove the crystallinity and texture of the sputtered TiO_2 thin film, X-ray diffraction was

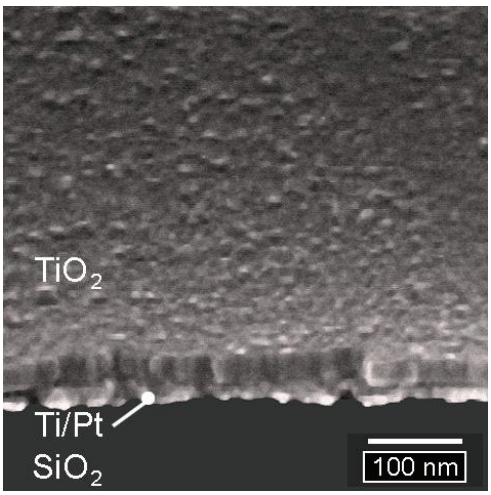


Figure 3.21: SEM cross section of a 30 nm thin TiO_2 film reactively sputtered on a Pt bottom electrode.

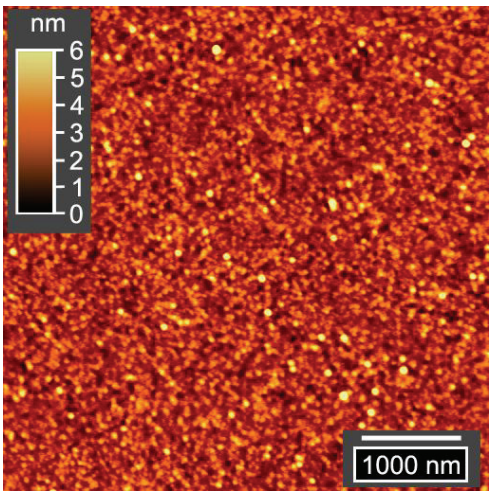


Figure 3.22: AFM picture of a 30 nm thin reactively sputtered TiO_2 film on a SiO_2 surface.

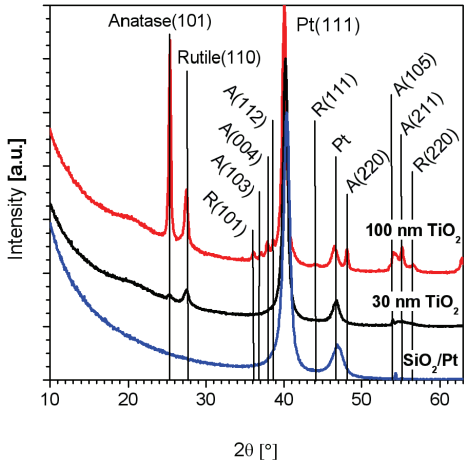


Figure 3.23: XRD of a 30 nm and a 100 nm thin TiO_2 film on a 30nm thin Pt electrode. The layer was measured by grazing incident angle diffraction.

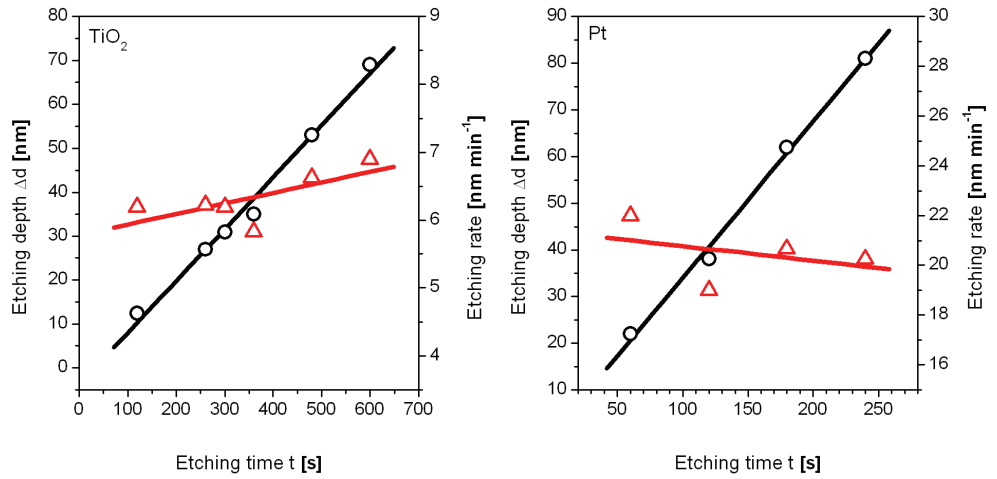
conducted to describe the pristine state of the functional layer. The measurement was carried out by grazing-incidence diffraction, which is most suitable for very thin layers [93]. The sample is irradiated by X-Ray under a constant incident angle, which is kept small to achieve a long path way through the thin layer, and to minimize the penetration into the substrate. Therefore, the sensitivity is enhanced. The incident angle for the presented measurements was $\omega = 0.5°$. The detector was moved in a 2θ range between 10° and 63° with an integration time of $200\ s \cdot 0.05°^{-1}$. Note that this type of measurement is an asymmetric one, meaning that also crystals that are not oriented parallel to the substrate surface are detected.

The result is shown in figure 3.23. The substrate was comparable to common samples and consisted of Si with a nearly 450 nm thin thermally oxidized SiO_2 layer. The back electrode was deposited by thermal evaporation and contained a 5 nm thin Ti adhesion layer with a 25 nm thin Pt electrode. This sample was measured to obtain the background signal (blue curve), which indicates clearly the Pt peaks at 40.05° and 46.51°. The black curve shows the X-Ray diffraction pattern for a sample with a 30 nm thin sputtered TiO_2 layer. The (101) anatase peak located at 25.36° had a small intensity contrary to expectation. However, a proportion of anatase is present, and its intensity increased for thicker layers. This is shown by the red curve corresponding to a measurement of a 100 nm thick layer that served as a control sample. In addition, rutile was observed, which is untypical for TiO_2 that was deposited near room temperature. The proportion of this phase also increases with the layer thickness just as the anatase. In comparison with the amorphous ALD-TiO_2 film, a distinct crystallinity with a columnar crystal growth was observed. This might influence the electrical characteristic of the material, among other things in terms of the electroforming properties.

3.5 Exposing the bottom electrodes

The use of dense and unstructured thin films of a functional material such as TiO_2 is a technical advantage because the memory cells in the form of crosspoint junctions require no additional alignment of the sandwiched layer. But large contact pads in regard to the device dimension, which are part of the bottom and the top electrodes, were used for the electrical characterization. As the bottom contact pads were also covered with TiO_2, this had to be removed by an additional etching process. An Ar^+ sputtering process was suitable for the removal of thin TiO_2 layers. The etching was performed by an Oxford Ionfab 300plus.

The anisotropic etching characteristic of this unit was suitable but not necessary for this application. The Ar^+ beam was aligned at an angle of 90° to the sample surface, which was rotated with 10 rpm for a higher homogeneity of the material removal. The process pressure was 10^{-2} mbar with an Ar flow of 10 sccm. The launched power for the etching was around 160 W.



(a) (b)

Figure 3.24: (a) Time dependent etch depth (black curve) and etch rate (red curve) for reactively sputtered TiO_2 and (b) for Pt.

The etching rate for TiO_2 was about 6 to 7 nm·min^{-1} and seemed to increase slightly for thicker layers as described in figure 3.24 (a). The increased etching rate over longer time periods might be explained by an increasing roughness of the material caused by the beam penetration and resulting in a larger working surface. To maintain an oxide free metal surface for the electrical characterization with the contact pads, the etching depth should be larger than the layer thickness. However, the Ar^+-milling is more selective for Pt films than for TiO_2 films with an etching rate between 20 and 21 nm·min^{-1}. The corresponding values are given in figure 3.24 (b). In combination with a good reproducibility of the layer thickness, the uncovering of the bottom electrode by a sputtering process was reproducible, too. However, the low selectivity for the TiO_2 opens a small time window for the over-etching.

4 Analytical methods for nano structures

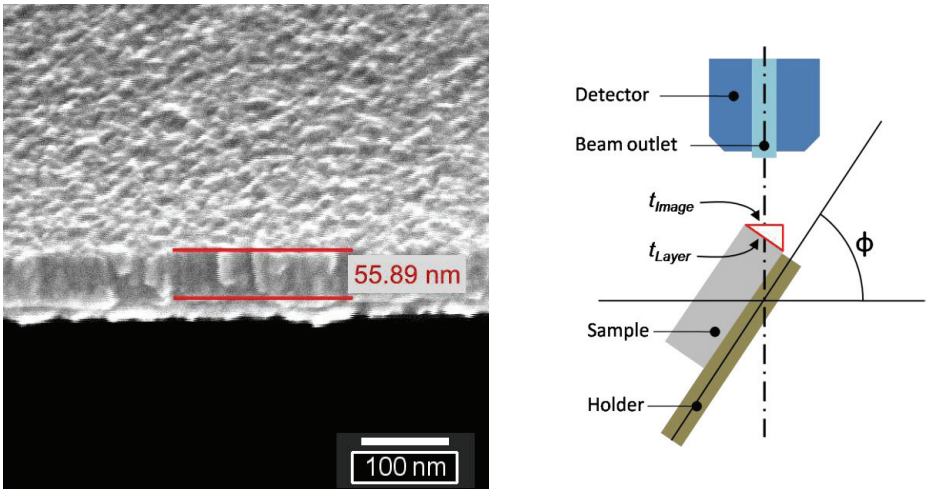
The examination of a nano crosspoint junction can be separated into two main topics, its geometrical setup and its electrical functionality, meaning its resistive switching characteristics. To examine and to describe the physical dimensions scanning electron microscopy and atomic force microscopy were used. Both are prevalent, well understood and described in a multitude of scientific literature and textbooks [94-97]. Still there were some aspects that have to be discussed in this study. To prove the application potential of the nano crossbar devices, a phenomenological electrical consideration was very important. Apart from that, the used electrical measurement setup and its properties will also be described within the following section. Material properties and related examinations were described by Jeong and can be found in [63].

4.1 Scanning electron microscopy for device examination

The general mode of operation of a SEM is comparable to the above described electron beam writer. An electron gun, normally constructed as a field emission gun, serves as the source and accelerates the electrons by a field up to 30 kV. Secondary electrons that are generated by the interaction between high-energetic electrons of the beam and atoms in the surface region are the origin of an image. The escaping secondary electrons have an kinetic energy of only several eV and are registered by a detector aside the electron beam outlet or an in-lens detector. Due to their low energy, only electrons descending from surface atoms account for the signal, which thus creates an image of the topography. Electrons from areas deeper in the material do not reach the surface since they lose their energy through scattering processes on their way to the surface. The intensity of the collected secondary electrons is than correlated with the beam position to generate an image.

A typical sample consists of an oxidized silicon substrate with a TiO_2 thin film sandwiched between two metal electrodes. Both oxides are highly insulating and not structured, which is why they create a high contrast to the metal structures during the examination of electrodes. To gain a better resolution, the acceleration voltage can be increased and the sample can be turned towards the detector to achieve a higher intensity by the secondary electrons. The gained resolution is then sufficient for the examination of the metal topography and normally used to image the steps of the top electrode over the bottom electrode. Details below 10 nm could be observed.

However, the excited surface material, which emits own electrons, appears to be self-luminous. The combination of shadowing effects, contrast of edges and rectification by the position control creates the illusion of an exchanged perspective between source and detector position. So, the surface relief of a nano device creates multiple shadings, which are frequently diffused by contrasts from different materials or charged areas leading to a misinterpretation of the obtained picture. An additional tool, such as the AFM (atomic force microscope), which is



(a) (b)

Figure 4.1: (a) Cross-section of a 60 nm thin TiO_2 layer for thickness determination. (b) Setup schematic for thickness determination. A typical angle is 70°.

described below, offers the information of the third dimension to interpret the measurements.

The SEM was used to determine the layer thickness of the TiO_2, which creates only a low but sufficient contrast to identify the interface at the SiO_2 as shown in figure 4.1 (a). The sample had been broken to obtain a cross-sectional view. For the inspection of samples, a Hitachi S4100 and a Zeiss Gemini 1550 were used. In general, both offered the same properties in regard of their applications. The Gemini 1550 was typically used for the layer thickness measurement. It was equipped with a detector that enclosed the beam outlet, as illustrated in figure 4.1 (b). So, the correction $t_{Layer} = \frac{t_{\mathrm{Im}age}}{\cos(1-\varphi)}$ results in a value for the real thickness.

Similar to the process of the electron beam direct writing, the penetration depth of the primary electrons is essentially larger than the thickness of the insulating layer. This is the reason why images of TiO_2 and SiO_2 are possible without a high resolution loss due to surface charges. Nevertheless, the beam current of the SEM amounts to several µA and influences therefore the electrical characteristic of a monitored device.

For taking micrographs of the resist structure, the sample was cooled down in liquid nitrogen before it was fractured. The polymer of the resist hardens extremely at this temperature and becomes brittle. The result is a sharp resist flank without any distortion caused by the mechanical strain, as shown in figure 3.8, 3.12, or 3.14.

Altogether, the SEM is a powerful tool to conduct the nano metal line analysis as a quality check in combination with the electrical characterizations described below. However, the current of the electron beam that penetrates the sample is in the µA range, which is comparable to the electroforming current that will be explained in the following chapter. From this point of view, the inspection of a virgin device might impact its electrical behavior.

4.2 Atomic force microscopy

The AFM measures the topography of a junction or metal line as well as the roughness of a surface. Both are essential information as they could have the same order of magnitude, resulting in a relevant influence by the roughness of the applied thin films. However; due to the lack of contrast, the AFM just shows the topography of the surface and gives no insight into the material arrangement.

In general, an AFM in ambient atmosphere, as the here employed SIS Picostation, was used in its intermittent mode. The cantilever with the probe tip is excited to oscillate around its resonance frequency. The amplitude of the oscillation as well as the phase is modulated by the distance between the tip and the surface due to the interaction of both masses. Thereby, the tip slightly touches the surface and is shifted up and down by its drive to follow the profile of the sample with a constant distance. The feedback signal that controls the height of the tip is used to render the surface, which is scanned line-by-line to gather the information of a complete plane.

Two different effects have to be considered for the interpretation of the AFM images: The first corresponds to the scanning speed of the system in $\mu m \cdot s^{-1}$. Schindler showed in her thesis that the measured roughness decreases with increasing speed [98]. For a low oscillation frequency of 100 kHz the number of oscillations per nanometer are in the range between 12.5 and 100 for common scan speeds between 8 $\mu m \cdot s^{-1}$ and 1 $\mu m \cdot s^{-1}$. This is a nearly atomic resolution and sufficient in ambient atmosphere. So, the cause for this dependency is rather the speed of the control loop for the height adjustment that creates an integrator for a constant measurement time. As a result, the system averages the surface profile with increasing scan speed. To obtain comparable results, the used scan speed was always 0.5 lines $\cdot s^{-1}$ each for 5 µm and 1 µm edge length.

The second effect describes the mapping of mesoscopic structures such as nano wires. As initially mentioned, the system performs measurements on the basis of the weak Van-der-Waals-interaction between the tip and the surface. The steep flanks of the nano wires with a height of several ten nanometers affected the oscillation comparable to the interaction with the horizontal surface. The result is nearly a mapping of the convolution between the sample and the tip profile as illustrated in figure 4.2. This results in a misinterpretation of the electrode profile in

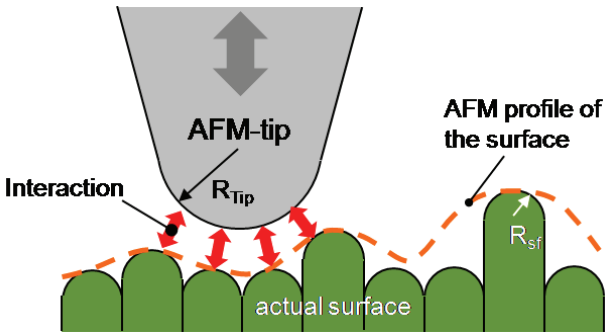
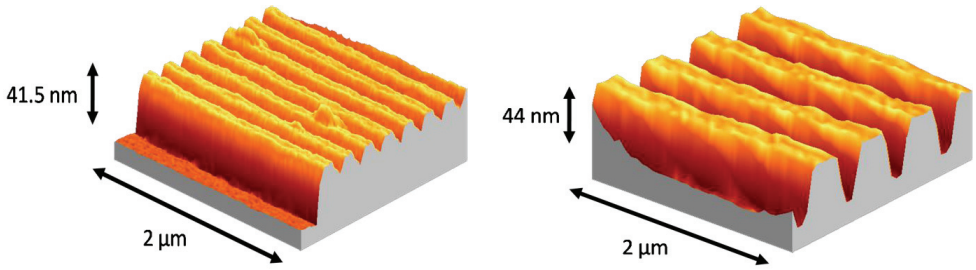


Figure 4.2: Scheme of an AFM tip scanning the surface and mapping the interaction of the surface with the tip profile depending on the structure size and the tip size [99]. The same effect creates erroneous images of nano electrodes as a result of the high aspect ratio.



(a) (b)

Figure 4.3: AFM scan of 30 nm thin Pt electrodes. (a) Incomplete mapping of the 100 nm wide gaps between two electrodes of the nano array bottom electrodes with 100 nm line width. (b) Mapping of an electrode set with 200 nm gap and line width.

an array structure, where several electrodes are arranged parallel to each other with a small distance. Figure 4.3 exemplifies the difference for a set of 200 nm and 100 nm wide lines with a distance of 200 nm and 100 nm, respectively. SEM examinations showed a gap/electrode ratio of nearly 1 and indicated therewith a complete insulation between the wires and their structural integrity. The probe tip of the AFM on the other hand cannot plunge into the gap due to the interaction with the sidewalls and reflects an incomplete isolation. In the case of a 200 nm wide gap the image shows the bottom of the structure but the distance is still wrongly interpreted in contrast to a SEM image. With this constriction, the AFM offers a microscopic insight into the roughness of the surfaces, also the top surfaces of electrodes. This helps to examine structural variations like spikes, hillocks and large grains that might affect the functionality of the devices as their dimensions are in the same range.

4.3 Electrical characterization

Besides the process technology, the backbone of this work is related to the electrical measurements. These served to prove the functionality and the characteristics of the fabricated structures by determining the resistance of the lines and the insulation between them. Additionally, the effect of ballistic charge transport in nano wires and the resistance switching in nano junctions was examined. They offered furthermore a proof of concept for the ease of integration of resistively switching materials into passive nano crossbar arrays and gave a first insight into the resistance switching of these devices.

Two different setups were used within this scope: A quasi-static one for the electrode structures without the functional material and the crosspoint junctions including it. To gain an insight into the performance, the latter were analyzed by a different setup with short pulses.

4.3.1 Setup for quasi-static measurements

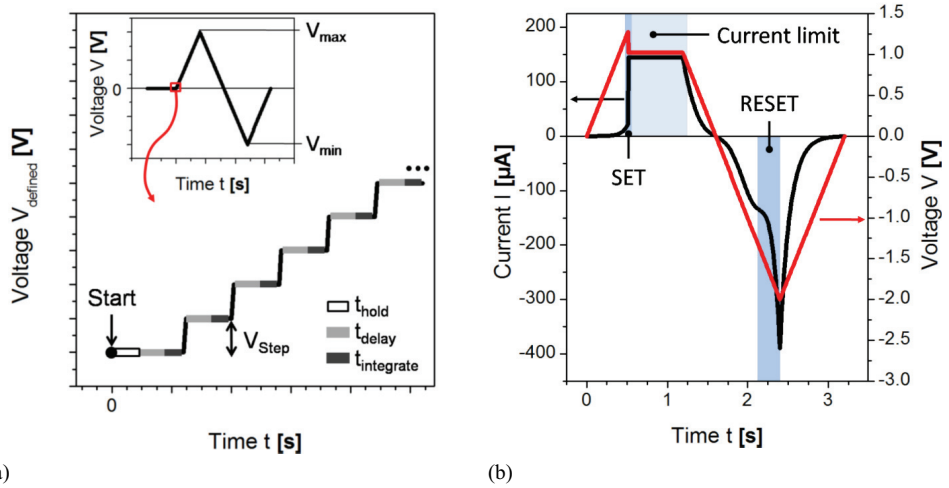
Quasi-static measurements are used to achieve the basic electrical parameters of devices such as the resistance of nano wires or their long-term characteristics under a certain current load. The generated signal can also be employed as control signal and constant or time-dependent voltage

or current function, respectively, to obtain an insight into complex device characteristics. However, the developing of the signal is incremental like a step function and not continuous. Each step is divided into the delay time and the integration time as illustrated in figure 4.4 (a). The former should be long enough to bring the sample in a static state after the preceding voltage jump. The integration time is used to obtain several measurement values, which are averaged to suppress noise. An optional function can be used to wait until the measured signal converges.

All quasi-static measurements were performed with an Agilent B1500A semiconductor analyzer, which was equipped with four source-measurement-units (SMU). This system offers a plain presentation of the switching parameters such as set- and reset- voltages and currents by a quasi-continuous $I(V)$ or $V(I)$ illustration. Crosschecks were performed with a Keithley 2600A SMU, which showed completely comparable results. However, the results are valid for the quasi-static case and might change drastically for dynamic excitations.

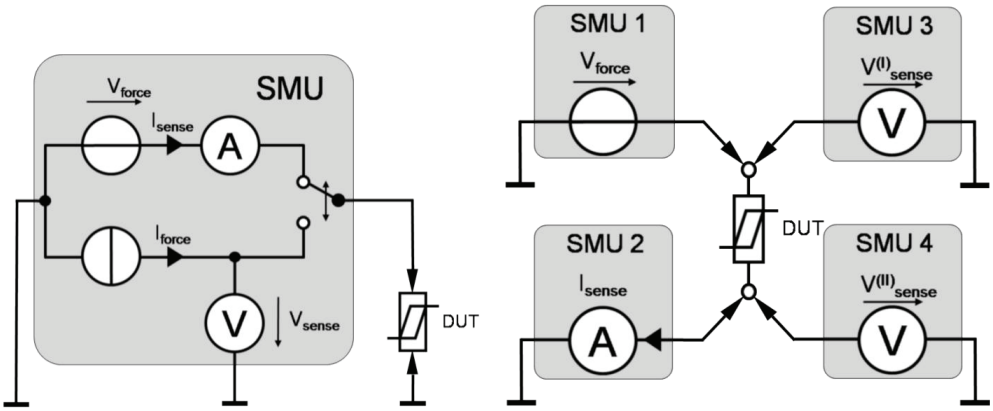
Most measurements were voltage controlled and performed by double bipolar triangular sweeps as shown in the inset of figure 4.4(a). The signal started at zero and increased until the predefined maximum voltage V_{max} was reached. Then, the voltage decreased to the minimum value V_{min} before it increased back to the zero-point. Additional parameters were the height of a voltage step V_{Step}, the delay time t_{delay}, the integration mode of the signal, which influences the integration time, and the hold time t_{hold}, which is the wait time between two subsequent measurements [100].

Another function is the current limit that protects the device from an overcharge. It reduces the voltage to an appropriate value when a certain current is exceeded. Thereby, the SMU tests every predefined voltage step by continuously checking the current. Whenever the current exceeds the selected limit, the voltage is reduced until the current falls below the allowed value. This is done for every predefined voltage even if the current limit was already reached. On the one hand, it offers the detection of a delayed resistance increase like a negative differential



(a) (b)

Figure 4.4: (a) Characteristic parameters of a voltage sweep. (b) Typical voltage curve and current response during a measurement with a predefined current limit. The corresponding $I(V)$ plot is presented in figure 4.6.



(a) (b)

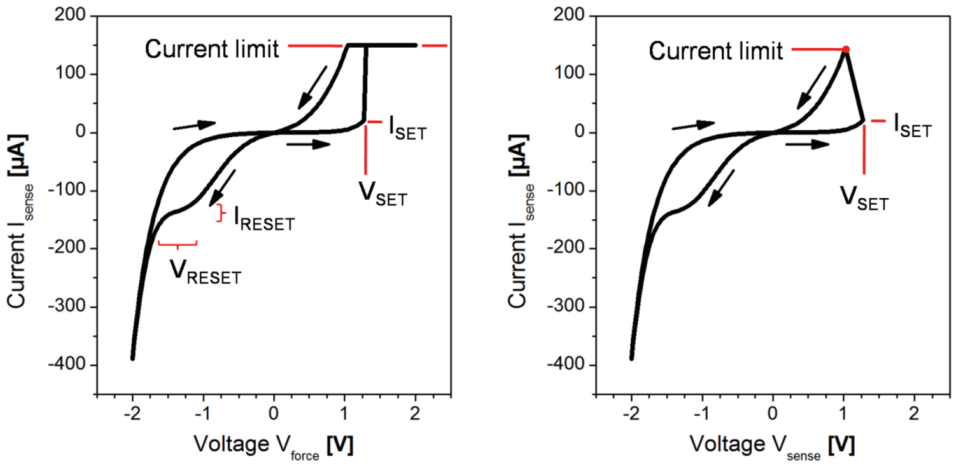
Figure 4.5: (a) Setup for a simple two-point measurement, showing a simplified circuit diagram of an SMU. (b) Four-point measurement setup with four SMUs, serving each as source, current or voltage measurement unit.

resistance. On the other hand, the source forces a high current load for a longer time period through the device, although this has already switched on and might be altered. To explain this and the therewith involved consequences, a plot of the voltage and the current over the time is shown in figure 4.4 (b). In the ideal case the voltage decreases and remains constant while the current is in its limit. Nevertheless, the current flows through the junction during the entire time that would be normally used to reach V_{max}, here 2 V.

In general, a two point measurement is adequate to characterize a two terminal device. The corresponding setup is demonstrated in figure 4.5 (a). Still, four-point measurements, schematically shown in figure 4.5 (b), offer two advantages. First, they give the contact resistance between the tungsten probe tip and the electrode. As the bottom electrodes had to be uncovered by dry etching, it was possible that thin residual layers of TiO_2 or resist were still attached to the electrode surface. This was normally mechanically and electrically broken by the pressure during the contacting and the very high electric field. Nevertheless, some probe tips tended to degrade the contact resistance due to contamination and eventually oxidation. So, a second probe for each pad, measuring the potential on the electrode, reveals this malfunction by comparing the force voltage of the source with the sense voltage as exhibited in figure 4.5 (b).

The second advantage of four-point measurements is the recording of the voltage values when the SMU is in the current limit. A typical two-point measurement records only the current response and plots this over the intended voltage as illustrated in figure 4.6 (a). The measured current response depending on the measured voltage, gained by a four-point measurement, is however shown in figure 4.6 (b).

Nano crossbar arrays consist of a large number of electrodes or metallization lines. The number of crosspoint devices is correspondingly larger. To dispose of a system that allows for the determination of devices in such a scale, a semiautomatic probe station, PA200 from Süss



(a) (b)

Figure 4.6: (a) Current response for a bipolar double voltage sweep plotted over the predefined control voltage. (b) Current response for a double voltage sweep plotted over the sensed voltage of a four-point- or a Kelvin probe measurement.

MicroTec was used. The electric drives of the chuck were able to move the sample automatically in xyz-direction. By defining two points along the x-axis of the sample, it could be aligned automatically by turning it around its centerline into a perpendicular position corresponding to the chuck axis. To perform measurements at elevated temperatures, the chuck could be heated in the range between 15°C and 200°C. Four fixed probe heads were available for the four-point measurements, which could be aligned initially. To connect the setup to a variable contact pad pattern of a crossbar array, an additional automatic probe head could be adopted. This could hold up to three probes with a fixed mutual position. With this setup four-point measurements or Kelvin-probing were possible, which could be performed on an arbitrary contact pad arrangement.

A darkbox shielded the setup against light and external electromagnetic influences. The system was controlled by the semiconductor analyzer. It was integrated into a mainframe that controlled the measurement programs, the server for the probestation and the heating system of the chuck. The electrical measurement was defined in routines, which could be concatenated in sequences. Additionally, routines and complete sequences were embedded into scripts. These also included the commands for the clients that controlled the chuck position and the temperature. A wafer map defined exactly the position of the contact pads, which could be approached by moving the chuck or the automatic probe. Then, the actual position was memorized and the measurements started. The results were monitored and saved in a file before the new position was specified by the actual position and the wafer map. The complete sequence was performed again until the repeat function reached a preset value. Several other options and a more detailed explanation are given by Rosezin [101].

These opportunities offer a wide range of semiautomatic applications. Beneath the presented testing of numerous electrodes, it is also possible to perform statistical surveys of the availability of devices depending on their parameters.

4.3.2 Setup for pulse measurements

To investigate the performance and the potential for resistance switching with short pulses, a different measurement setup was used. The write operation was performed by the Agilent pulse-pattern- generator 81110A whereby the signal was controlled directly via Kelvin-probing, using a Tektronix TDS6804B oscilloscope. The read-operation of the information was conducted by a SMU from the semiconductor analyzer as a fast reading did not contribute to an insight into the switching performance. Additionally, a quasi-static triangular read signal was easier to control [102]. The setup of the probe station was the same as for the quasi-static measurements, but the type of the probe tip had to be selected concerning the bandwidth of the application. A coaxial tungsten probe tip was used to ground the bottom electrode of the device, and a second one was connected with the SMU for the read operation. A third triaxial probe was shielded up to a short tip and offered a bandwidth of 3 GHz that was sufficient for pulses with a duration of 10 ns. Additionally, they had two connectors for a Kelvin-probing setup allowing for the simultaneous measurement of the applied signal at the probe tip on the contact pad.

The setup is illustrated in figure 4.7 whereby the switching between the writing and the reading section was normally performed with an exchange of the corresponding probe tips. The procedure starts after the electroforming of the device, which is described in chapter 5. By approaching the RF-frequency probe to the top electrode and triggering a single pulse, the device is written. Then the SMU for the reading is connected and a measurement is carried out to determine the resistance state. This is repeated for every writing / reading sequence. The pulse can be adjusted in regard of its amplitude, polarity and duration. Also complete continuous patterns of pulses can be applied to examine the device. The simple combination of a set-pulse followed by a read-sweep, a reset-pulse and finally again a read-sweep demonstrate the potential for the use of the device in a real application as pulses are typically used to control the devices of a CMOS-application. A current limit was however not available and, as shown later, not necessary.

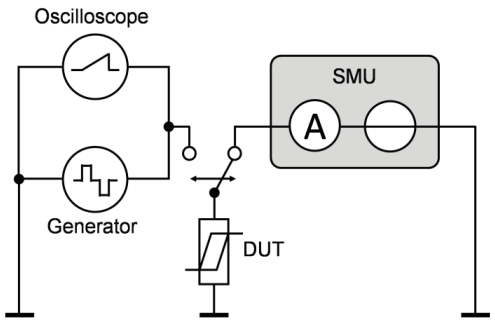


Figure 4.7: Pulse measurement setup with a combination of a generator and oscilloscope for the writing and a quasi-static SMU for the reading of the information.

5 Nano electrodes

The following chapter describes the electrical properties of nano metallization lines, starting with a brief introduction of the incorporated metals. To examine in how much scattering effects concern nano lines in crossbar arrays and to give an outlook for future integration aspects, test patterns and their electrical characteristics are presented. These results are compared to the fabricated nano devices that serve as template for the integration of functional materials. Finally, single nano crosspoint junctions, word structures and crossbar arrays including their supply lines are described and discussed.

5.1 The choice of the electrode material

At first sight, the conductor of a crosspoint junction forms the connection between the contact pads or vias and the junction itself. In this case, the material is subject to the requirements for a good conductor that serves as a supply line. This aspect will be regarded in chapter 6 focusing on long wires with a profile in the nanometer range. Here, the described devices were examined in terms of material issues, because the electrodes may become part of the resistive switching effect. From several authors it is known that Cu and Ag favor the creation of filaments in a matrix of chalcogenide glasses or SiO_2 [26, 68, 103, 104]. The effect of diffusing metals in TiO_2 is not fully understood, but comparisons with corresponding measurements suggest the formation of metallic filaments [92]. However, the establishment of metallic filaments was in this context not the intention for the use of TiO_2. As the switching of TiO_2 in combination with two inert electrodes was already demonstrated, this could lead to the superposition of two possible but different switching mechanisms. Both effects combined in one system were expected to implicate a loss of reproducibility of the resistive switching parameters and lead to a very complex control system for the read and write procedures. That is why well-conducting and potentially diffusing materials like Ag and Cu are excluded as electrode materials, although their incorporation is technically possible. Au is the third material that tends to diffuse into layers where it changes the electronic properties of the functional film, even though no electrochemical Au switching-cell has been observed so far.

The intended mechanism is assumed to be induced by the reduction and oxidation of the TiO_2 film and the migration of oxygen and its vacancies, respectively. Due to these chemical reactions that are fundamentally influencing the electrical behavior of the cell, base metals like Al or W that are used in semiconductor processing industry were unfavorable during the initial examinations. These could lead to the formation of Al_2O_3 or WO_x increasing the complexity of switching systems. As already mentioned, first examinations related to resistance switching, performed by Jeong [63], showed good results for Pt as electrode material. However, the higher resistivity of $\rho_0 = 10.5 \cdot 10^{-8}$ Ωm of Pt is a compromise for its partly chemical inertness. As the asymmetry of accumulation and depletion of oxygen vacancies along the interfaces is assumed to

support the switching, an additional Ti interlayer was used between the TiO_2 and one of the Pt electrodes. The Ti was patterned, as described in the next section, like the Pt electrode to obtain a good insulation between two neighboring devices.

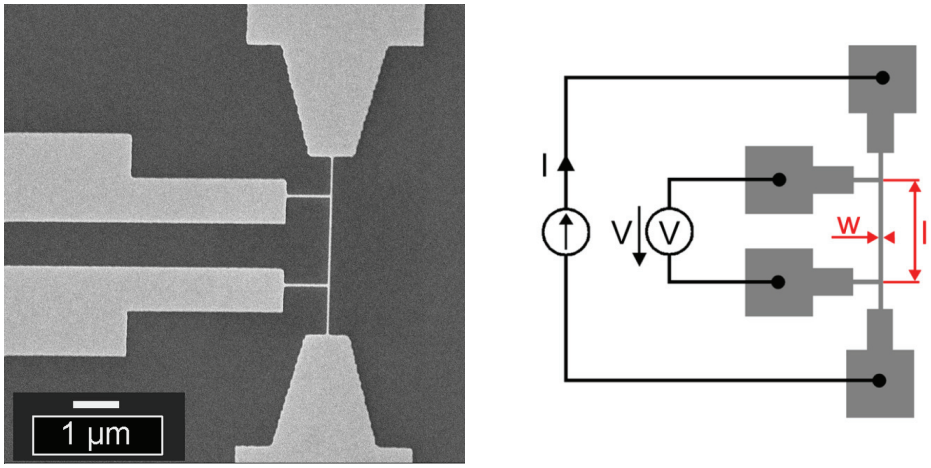
5.2 Test structures

To get an insight in the property of nano devices and metallization lines, particular test structures were fabricated. These were designed according to the special requirements for high precision resistance measurements.

Reliable results could be obtained by four point bridge-like structures [105]. Figure 5.1 (a) shows a SEM picture of the test device with a 100 nm wide conductor. The corresponding application is illustrated in figure 5.1 (b). A current sweep starting at 0 and increasing up to 25 µA is induced by the upper and the lower supply line. The sense contacts at the left side were connected with a voltmeter, measuring the voltage drop over a predefined nano line. Since the input impedance of the voltmeter was very high (10^{13} Ω), the voltage drop along the metallization line was only caused by the current flow through the section of the connected line. This is determined by its width w_{cd} and its length l_{cd} leading to the sheet resistance R_s

$$R_s = \frac{V}{I} = R \cdot \frac{w_{cd}}{l_{cd}} \left[\frac{\Omega}{\square}\right]. \qquad (5.1)$$

All fabricated wires had a length of 2 µm and a width between 40 and 200 nm. The used electrode material was a stack of 5 nm Ti and 25 nm Pt yielding a precise value for the resistance per junction section in a crossbar array. Poly-crystalline platinum bulk samples have a resistivity of $9.8 \cdot 10^{-5}$ Ωm [106]. However, layers that are fabricated by electron beam evaporation could not achieve this value. The reasons were inhomogeneities within the morphology and process induced impurities. In the following, the electrode resistivity is normalized by the bulk value to obtain a significant value for its quality.



(a) (b)

Figure 5.1: (a) SEM figure of a bridge structure for the determination of the sheet resistance of nano lines. (b) The corresponding four-point measurement setup.

5.3 Electrical characteristics

The following values present the median of a set of measurements each performed at Pt conductors with different width but the same fabrication parameters. With the use of equation 5.1 and the predefined geometries the resistivity was calculated, whereas the Ti adhesion layer was neglected. This was tolerable as the layer was very thin and its bulk resistivity of around $40 \cdot 10^5$ Ωm was more than four times higher compared to Pt.

Figure 5.2 presents the increase of the resistivity depending on the wire width of an as-deposited sample. The metal structures were applied on an oxidized Si substrate, which was common for all presented applications. With a normalized resistivity of around 3, extrapolated for a larger wire width, the resistivity of the thin film is essentially higher than the ideal one. The reason could be found in the 25 nm thin metallic film that is in the range of the mean free path. The approximation for the R_{gb} and p were performed with a least squares fit, whereas the grain size d_g was assumed to be constant or scaling linearly with the wire width.

An additional reason was found in the mesoscopic fluctuation of the line width due to shape variations of the developed resist. The predefined and fabricated width was an average value that applied for classical considerations. In this case, the higher resistance of narrow conductor sections would be cancelled by wider sections. But theoretical considerations show a nonlinear dependency between line width and resistivity due to an increase of the sidewall scattering and decrease of grain size. As a result, narrow sections have a higher impact on the total resistivity than wider ones, which is described by the line edge roughness (LER) [107]. Larger devices with wire dimensions of more than 100 nm show only a small dependency, whereas the value increases drastically for smaller dimension. A fit for the examined values with a constant grain size of 10 nm indicates clear deviations for the parameters $p = 0.4$ and $R_{gb} = 0.2$, which presented nevertheless the base case. The therefore used function is described by equation 2.12. A more meaningful result could be obtained by assuming a dependency between the wire size and the grain size, as already observed by Durkan et al. [45, 108]. In this case the simple assumption was made that the grain size scales linearly with the wire width with a factor 0.1. The resulting fit is also given in figure 5.2 with the parameters $p = 0.25$ and $R_{gb} = 0.075$, and presents a better correlation with the measurements. However, the used parameters are only an approximation resulting in a better fit for the measured values and are therefore only valid with restrictions [109]. The difference between the fit with constant grain size and variable grain size led to the examination of the real grain size. This was estimated by SEM pictures of nano electrodes with different widths. The observation of SEM images offered room for conjecture but averaging several diameters led to the dependency of $d = 4\ \text{nm} + 0.057 \cdot w$ for wires that are broader than 50 nm. The corresponding fit is shown in figure 5.3. For larger wires, the given linear dependency between the width and the grain size allowed an adequate estimation. But the deviation became large for smaller wires, whereat SEM observations were not reasonable for smaller widths leading to no further insight into the morphology of the wires.

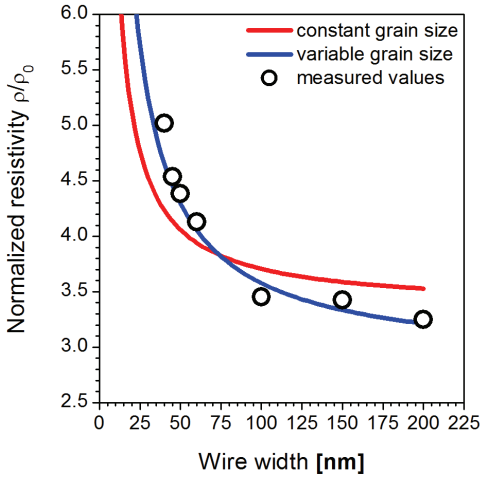


Figure 5.2: Resistivity of a 25 nm thin Pt wire depending on the lateral size. The red fitting curve is subject to constant, whereas the blue one corresponds to variable grain sizes.

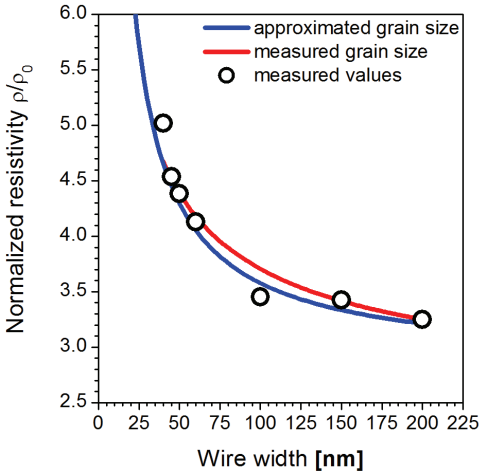


Figure 5.3: Difference between the assumed grain size (blue) and the determined grain size (red).

The second experiment deals with the influence of a Ti/Pt/TiO_2 stack underneath the electrodes, which is partially the case for the fabricated top electrodes. The thicknesses of the single films corresponded with 5, 25, and 30 nm to the dimensions used for the investigated structures. In general, this material system exhibited a higher roughness compared to SiO_2 surfaces, which is why an increase of the resistivity was expected. The results are shown in figure 5.4 and compared with the values measured and fitted for structures on SiO_2. To at least gain a qualitative approach for the comparison between the influence of

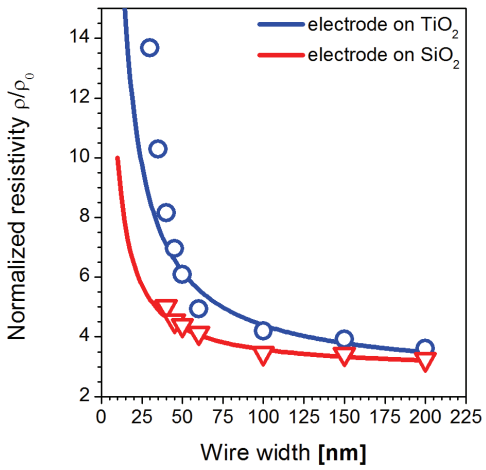


Figure 5.4: Resistivity dependence on the wire width for a top electrode on a flat TiO_2 surface (black circles). The blue fitting curve was gained with the parameters $p = 0.15$ and $R_{gb} = 0.3$, whereas the red curve and measurement values are consistent with Fig. 5.2.

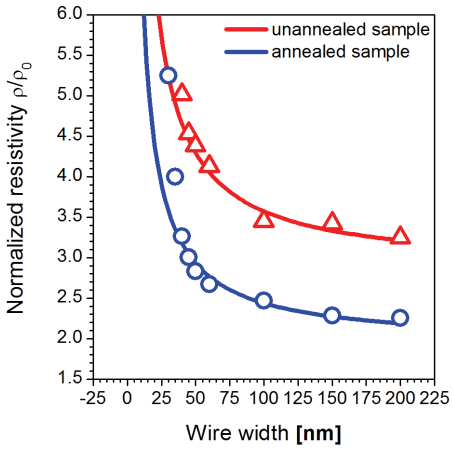


Figure 5.5: Resistivity of annealed wires (blue circles) compared to untreated wires (red triangle and red curve). The fitting parameters for this results are $p = 0.65$ and $R_{gb} = 0.075$ (blue curve).

a TiO_2 and a SiO_2 substrate, both curves were calculated by the approximation with a linear grain size dependency with the factor 0.1. A determination of d_g by SEM or AFM was not possible, because the topography of the metal surface included a reproduction of the interface topography with the substrate.

The measured resistivity was slightly increased for wide and considerably increased for narrow electrodes. In general, the fitting parameters indicated a higher degree of diffuse reflection along the side walls and a higher impact by grain boundary scattering. Additionally, the roughness of the TiO_2 surface affected the mesoscopic roughness of the metal lines. This effect advanced for narrow metal lines when their physical dimensions approached the dimensions of the TiO_2 surface roughness. For electrode widths above 50 nm, which were typically used within this study, the resistivity increase was within the limits of the general tolerances. That means that different effects such as switching parameter deviations would have been relevant for the operation of a nano device. However, future applications with pattern sizes of only several nanometer demand a plane surface to avoid high resistivity differences between top and bottom electrodes.

The final experiment clarifies the impact of excessive heat on the resistivity of nano lines. This was done related to experiments with unstructured, platinized substrates. Here, it was observed that an annealing step reduced the occurrence of hillocks. Based on this insight, it was assumed that an additional annealing process might reduce the microscopic and mesoscopic roughness of the wires. Therefore, several samples were annealed at temperatures up to 600°C in a nitrogen atmosphere. Figure 5.5 presents the results from a sample that was annealed at 425°C for 60 minutes. In comparison with an untreated sample, the resistivity decreased for about 30% showing an advantageous effect. Also the parameters p and R_{gb} indicated a higher quality of Pt because p changed from 0.5 to 0.65 indicating a higher specular reflectivity at the sidewalls. R_{gb} decreased from 0.175 to 0.075 due to a lower impact by the grain boundaries. The same effect and gain was observed for higher temperatures up to 600°C and also for Pt electrodes on a TiO_2 surface.

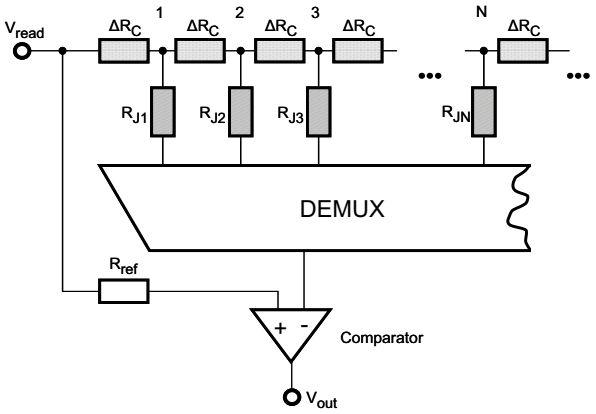


Figure 5.6: Scheme of a single row of resistive switching junctions and its related conductor resistances. The figure shows exemplarily the left part of a symmetrically controlled conductor from the outermost to the central storage cell. Depending on the ratio between R_{ref} and the overall resistance within the structure, the comparator interprets the stored information as logical '1' or '0'.

An increase of the resistivity, caused by a diffusion of Ti from the adhesion layer into the grain boundaries as described by Schmidt et al., was not observed [110]. If this had been the case, the corresponding effect would have been overcompensated by the improvement due to the thermal treatment. To estimate whether these Pt wires are suitable for the integration of TiO_2 into passive arrays or not, a simple model is used. This anticipates the switching parameters that will be given in the next chapters. However, any increase in resistivity will decrease the maximum array dimension according to the conclusion by Mustafa et al. [32]. For simplification a single row as described in figure 5.6 is contemplated in the following. All parasitic currents that would affect the evaluation additionally in the case of an array are neglected. Given a material with resistance values R_J of 100 kΩ and 1 MΩ for R_{ON} and R_{OFF}, a feasible decision boundary between these states would be R_{ref} = 550 kΩ. The additional resistance due to the connecting conductor in comparison to a device at the border of the array should be less than 450 kΩ. Any larger value would lead to a false "high resistance" interpretation within this concept for a low state in a central junction. If the distance Δl between two adjacent junctions fulfils the condition $\Delta l = 2 \cdot w$, the proportional conductor resistance for every additional element in a row is given by

$$\Delta R_C = \rho(w,t)\frac{\Delta l}{w \cdot t} = \rho(w,t)\frac{2}{t}. \tag{5.2}$$

The dependency of the resistivity ρ on the conductor dimensions w and t can be solved by the normalized resistivity in form of a size factor $a = \rho/\rho_0$ (figure 5.2 to 5.5) for

$$\Delta R_C = a \cdot \rho_0 \frac{2}{t}. \tag{5.3}$$

The maximum number of junctions N_{max} for the ideal case of a platinum conductor with a thickness of 25 nm and a width of 100 nm would be around 30,000, deduced by the condition $N_{max} \cdot \Delta R_C < R_{ref} - R_{ON}$, described in figure 5.6. This estimation considers the mirror symmetry with operating voltages at both conductor terminations, which doubles the size of a row. As a result, the maximum number of devices is inversely proportional to the size factor a, and the number of devices decreases to around 22,000 for a conductor width of 25 nm.

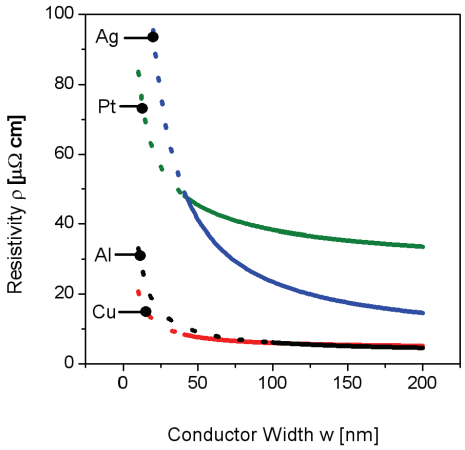


Figure 5.7: Resistivity over metallization line width for different evaporated materials.

Any scattering in the resistance levels as well as the consideration of interacting junctions within the network of a passive array will reduce the maximum array size. Nevertheless, these theoretical numbers clarify that the resistivity of the Pt electrode is sufficiently low and will not become a limiting factor.

A further decisive factor is the erase voltage, which has to be exceeded to switch the junction from the ON- to the OFF-state. A purely resistive network forms a voltage divider between the involved connection lines and the addressed junction. For the given example, the erase voltage increases by a factor 5.5 for the central storage cell. Depending on the maximum feasible supply voltage and the required erase voltage, this represents a higher restriction for the array size in regard of the electrode resistances. Assuming a more realistic and controllable device size with 128 bit in the given model would lead to a supply line resistance of nearly 3 kΩ and 2 kΩ for the central junction in 25 nm and 100 nm large structures. The corresponding power loss for a switching current of 100 µA would be 30 µW and 20 µW in comparison to about 200 µW power consumption of the cell. A suitable value for the LRS is 10 kΩ, which leads to an increase of the ratio between total supply and switching voltage of 1.3 and 1.2, respectively, for the worst case of a reset-procedure.

Additional materials such as Cu, Ag and Al were incorporated into nano test structures and electrically characterized [101]. Figure 5.7 shows the fitted curves for the resistivity depending on the wire width for a 25 nm thin electrode. Cu lines exhibited the best scalability, because its resistivity and the size effect are low. However, a passivation layer is necessary to prevent diffusion and the corresponding effect on the resistance switching is unknown. Good results were also achieved for aluminum lines that were wider than 100 nm. Smaller electrodes however showed significantly more defects or very high resistances. As the test-devices were exposed to ambient atmosphere the oxidation to Al_2O_3 might have affected the lines with their small physical dimensions. A comparable property was observed for Ag electrodes, which were subject to a high size effect. In this case, the generation of AgS_2 in ambient atmosphere might be

the reason as well as an inappropriate metal structure. In this context, Pt has a disadvantageously high resistivity compared to copper. However, it suits the demands of a resistively switching TiO_2-system without any additional passivation. It is stable in ambient atmosphere and shows good scaling properties.

A downscaling by the factor 4 from 100 nm to 25 nm would lead to an increase of the resistance by a factor 1.25 to 1.5. Additionally, the resistance per junction section is orders of magnitude lower than the LRS. From this point of view, Pt is a suitable metal for nano crossbar arrays with the potential for a further size reduction.

5.4 Design and features of nano crosspoint junctions

The next section describes the design and the properties of the fabricated nano structures that were used to examine the resistive switching properties of TiO_2 in nano crosspoint junctions. The presented devices can also serve as templates for several other materials that are not subject to an epitaxial growth or which need an especially textured electrode that cannot be fabricated by a lift-off or etching process.

Three different types of devices were designed and fabricated. The first one was an isolated single nano crosspoint junction that was used to prove the scalability of the resistively switching material into the nanometer range. The second device was a so called word structure. The name describes the assembly and connection of the storage cells that were created by a single top electrode crossing a set of parallel bottom electrodes. A complete use of all cells corresponds to the storage of a word, double word or quad-word etc. This structure could also be called a $1 \times n$ array. The third device type, which was investigated, was an $n \times n$ array, containing as many top as bottom electrodes. These crossed each other perpendicularly. Whereas word memories served for the examination of the interaction of adjacent junctions within one dimension, arrays opened up a plane. This does not only correspond to geometrical but also to electrical considerations as these structures offer several opportunities for bypasses.

Figure 5.8 is a SEM picture of a complete pattern, containing an 8×8 bit array in the center and single junctions in the upper corners. Other patterns contain a word, and in larger structures over 16 bit the single junctions were removed to keep the number of pads below 36. The contact pads, which have a size of $100 \cdot 100\ \mu m^2$, are positioned around the outer border of the structure.

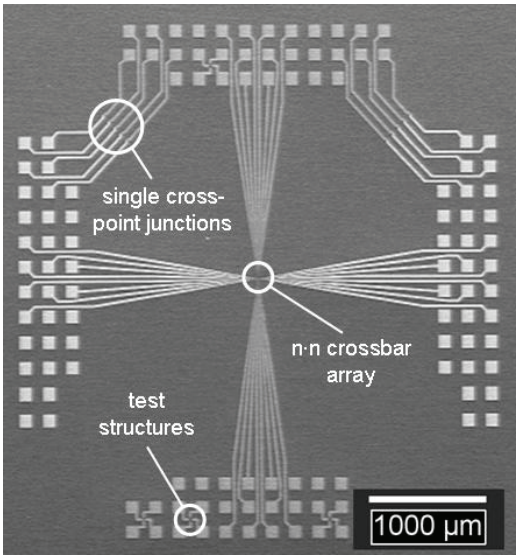
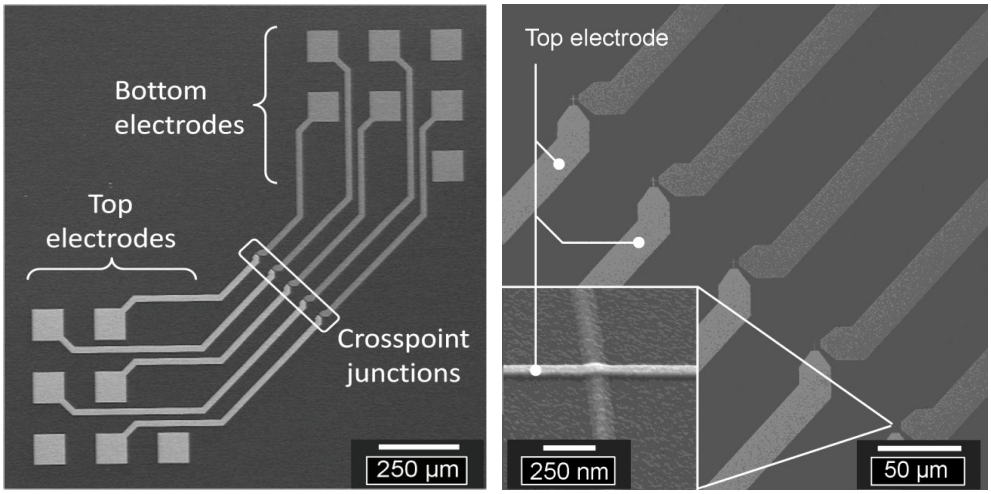


Figure 5.8: Complete pattern of an 8 bit nano crossbar array with 100 nm half pitch.

5.4.1 Single nano crosspoint junctions

Single nano crosspoint junctions were fabricated with five different wire widths. The largest one was 500 nm wide, the others scaled down to 100 nm in steps of 100 nm. The SEM picture in figure 5.9 describes the design of the fabricated electrodes. The contact pads are arranged in a row of three at the outer border of the pattern. This result in longer interconnecting wires that lead to the junctions. The advantage is a higher symmetry of the pad arrangement, which simplifies an automatic probing.



(a) (b)

Figure 5.9: (a) Pattern of single crosspoint junctions with supply lines and contact pads. One set consists of five devices with sizes from 500 · 500 nm² in the upper left corner to 100 · 100 nm² in the lower right corner. (b) Detailed view of single crosspoints.

A set of devices was fabricated on top of a TiO_2 sample, but comprised no functional TiO_2 thin film in the junctions. These were used to determine the resistances of the interconnect lines between the contact pads without the influence of the resistively switching material. Nevertheless, the thin metal layers generated a serial resistance, which is essentially higher than that of the electrodes in capacitive stacks or in small micro crosspoint junctions. The measured values are given in table 5.1. Additionally, the corresponding length of one half of the supply line is given.

Table 5.1: Dimensional and electrical values for single junction supply lines.

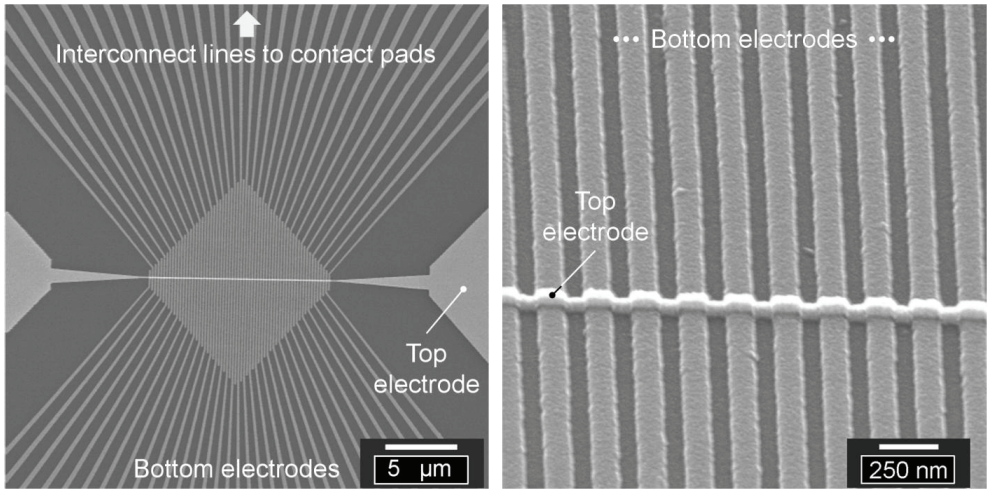
Cell size [nm²]	Wire length [µm]	Measured resistance [Ω]
100 × 100	802.81	1532
200 × 200	956.52	1295
300 × 300	661.39	889
400 × 400	815.10	1018
500 × 500	519.97	677

5.4.2 Nano words or register like structures

The second kind of devices were the above mentioned word structures. These were designed and fabricated with half-pitches of 200 and 100 nm. The storage sizes were 8, 16, 32 and 64 bit. Figure 5.10 shows a 64 bit word with 100 nm half-pitch. In devices up to 32 bit, the wires connect the upper and the lower contact pads and provide an electrical inspection of its properties. The supply lines had therefore a wedge-shaped form with an increasing width between 100 nm or 200 nm and 20 µm to reduce the resistance as much as possible. The length of the top electrode corresponded to the width of the set of bottom electrodes plus 500 nm on each side as alignment tolerance. A single top electrode of a word structure was comparably long but was not affected by adjacent structures. Therefore, the influence of the substrate surface was examined in the manner of the test structures in the previous section. Three different types of samples were prepared with the same lift-off metallization process on different substrates. The first one was a SiO_2 surface, which was normally used for bottom electrodes. The second one contained only a 30 nm thin reactively sputtered TiO_2 layer, and the third one was the typical combination of a bottom electrode covered with the TiO_2 layer. The dimensions of the fabricated nano sized metallization lines are summarized in table 5.2.

Figure 5.11 presents the measured resistances R_{te} for the three samples that were mentioned above. The word top wire on the SiO_2 shows the lowest values in average. The complete wire with the length l_{te} for the 100 nm 8 bit word has a resistance of 1360 Ω scaling up to 3100 Ω for the 64 bit structure and 1157 Ω up to 2440 Ω for the 200 nm wires, respectively. This enables the estimation of the resistances for the interconnection and the nano electrode by the equation

$$R_{te} = \rho_{itc}\frac{l_{itc}}{w_{itc}\cdot t_{metal}} + \rho_{nw}\frac{l_{nw}}{w_{nw}\cdot t_{metal}} = R_{itc} + \frac{\rho_{nw}}{w_{nw}\cdot t_{metal}} l_{nw}. \tag{5.4}$$



(a) (b)

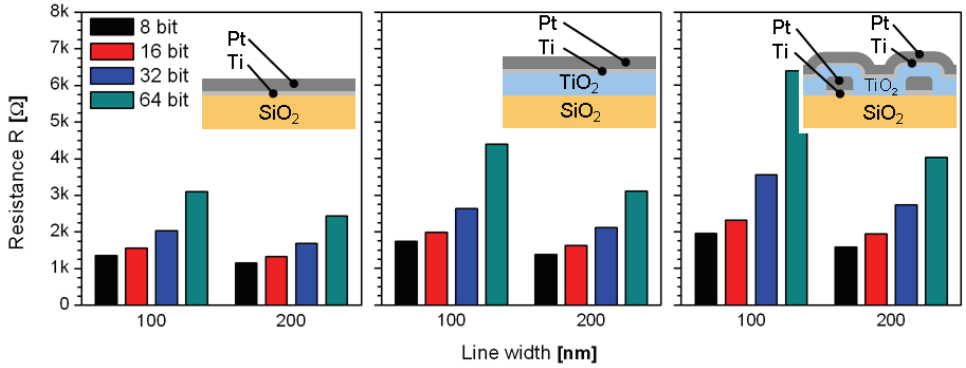
Figure 5.10: (a) SEM picture of a 64 bit word structure with 100 nm wire pitch. On the right and the left side is the 20 µm wide supply line for the top electrode. (b) Detailed view of the word electrodes showing the arrangement of the top over the bottom electrode.

Table 5.2: Length of the nano metallization lines in the center of the device. The overall length of the metal wire between the contact pads amounts to 3900 µm.

Word size [bit]	Width of wire [nm]	
	100	200
	Metal line length [µm]	Metal line length [µm]
8	2.5	4
16	4.1	7.2
32	7.3	13.6
64	13.7	26.4

We can consider the resistance of the supply wires, e.g. interconnect wires to be constant because $l_{itc} = l_{te} - l_{nw}$ but $l_{te} \gg l_{nw}$. This led to the result that the average interconnect resistance is 928 Ω for the 100 nm and 917 Ω for the 200 nm wide structures. The resistance of the nano lines scales with 157 $\Omega \cdot \mu m^{-1}$ and 57 $\Omega \cdot \mu m^{-1}$ for the 100 nm and the 200 nm wide wires, respectively. The ratio of the resistivity is 1.38, which is not in the range between 1.11 and 1.14 predicted by the Fuchs-Sondheimer model.

The measured values for the word electrode on the TiO_2 were substantially higher with: 1730 Ω to 4390 Ω (for 8 bit to 64 bit) for the 100 nm and 1380 Ω to 3100 Ω for the 200 nm wide lines. The resistance on the TiO_2 increased between 28% and 42% compared to the SiO_2 substrate for the 100 nm wide structures and between 20% and 27% for the 200 nm structures, respectively. An explanation is the increase of the resistivity due to the rough surface of the TiO_2 layer underneath the electrode, which increased the microscopic and the mesoscopic roughness and the therewith associated influences of the sidewall scattering as well as the LER. Additionally, a change in the size and morphology of grains could increase the resistivity. Here, the resistance per length was 225 $\Omega \cdot \mu m^{-1}$ and 76 $\Omega \cdot \mu m^{-1}$ for the 100 nm and the 200 nm



(a) (b) (c)

Figure 5.11: Top electrode resistance for word structures of 8, 16, 32, and 64 bit with 100 nm and 200 nm wide wires each. (a) A standard Ti/Pt electrode on unstructured SiO_2 (b) Resistance of a top electrodes on a TiO_2 film without any bottom electrode, and (c) for a complete word structures with a set of 8, 16, 32, 64 parallel bottom electrodes covered with a TiO_2 film.

wide lines, respectively. This effect became stronger for the complete word structure where the top electrode covered a set of bottom electrodes in combination with a thin TiO_2 film. The average resistances per length were 385 $\Omega \cdot \mu m^{-1}$ for the 100 nm and 109 $\Omega \cdot \mu m^{-1}$ for the 200 nm wide wires, respectively. Here, two additional reasons for the increase occurred. The top electrode became effectively longer as it had to follow the topology of the patterned bottom electrode and TiO_2. Furthermore, the metal deposition was not isotropic, which is why constrictions along the step edges had to be considered (see figure 5.11 (c)). Also the estimated values in regard of the 20 µm broad interconnect wire increased to values between 1070 Ω and 1180 Ω for the TiO_2 covered sample.

As mentioned in chapter 3, the deposition of metal was subject to slight deviations of the material thickness. Even though this effect was small, it was amplified by the ballistic effects described above. For this reason, all values given in this section contain a certain error but were a very good representation of the occurring tendencies and demonstrate well the achieved magnitudes.

Devices with less than 64 · 64 junctions have a continuous wire from the upper contact pads to the lower contact pads and could thus be checked with regard to interruptions within the conductor. Additionally, it was possible to measure the occurring resistance of each supply line. Due to the symmetry of the pattern, it is possible to deduce the external resistances for each junction, which is nearly half of the determined values neglecting any inhomogeneities and asymmetries in the very center. This is valid, as the latter presented finally only a fraction of the total resistance. Furthermore, each junction was addressable from both sides, which offered some redundancy to bypass interrupted wires.

Figure 5.12 shows the resistance pattern for the 8, 16 and 32 bit large word devices with 100 nm half-pitch. The same is shown for the 200 nm devices in figure 5.13. Like the pattern itself, the results are mirror-symmetrical as expected. Remembering figure 5.10, the inner nano lines are longer than the outer ones, which should be reflected by the resistances. But this effect is compensated by the wedge-shaped interconnect lines, which are accordingly longer for the

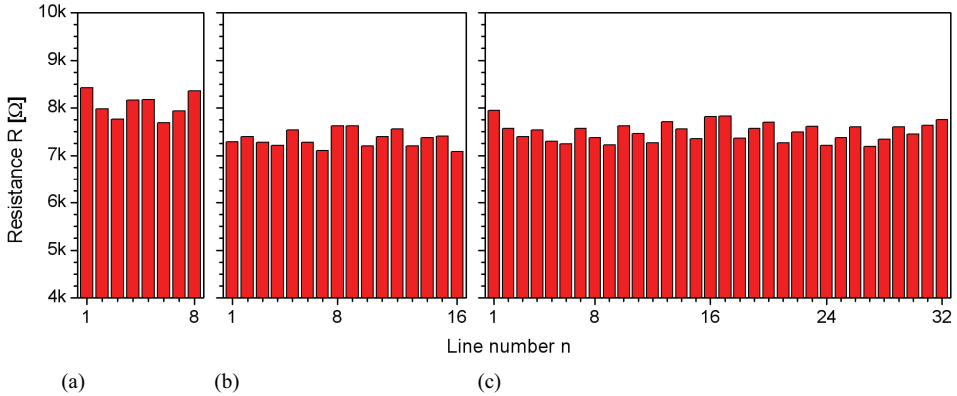


Figure 5.12: Resistances of the complete set of metal lines consisting of the central nano electrodes and the interconnect lines. Shown are the distributions for the 100 nm wide (a) 8 bit, (b) 16 bit and (c) 32 bit word devices.

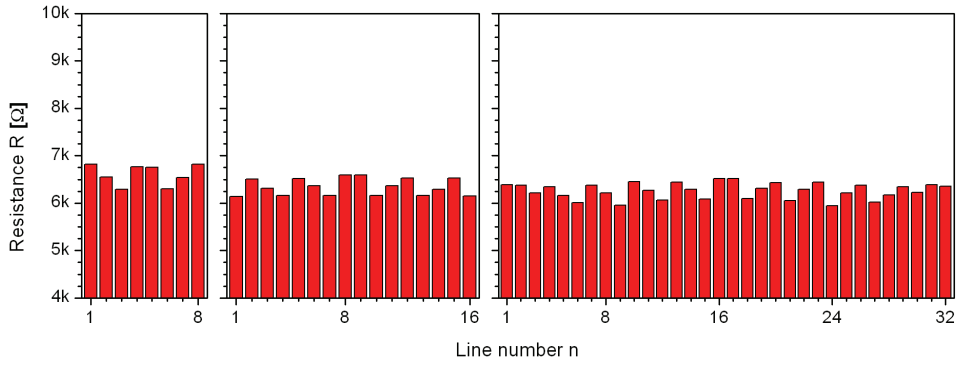


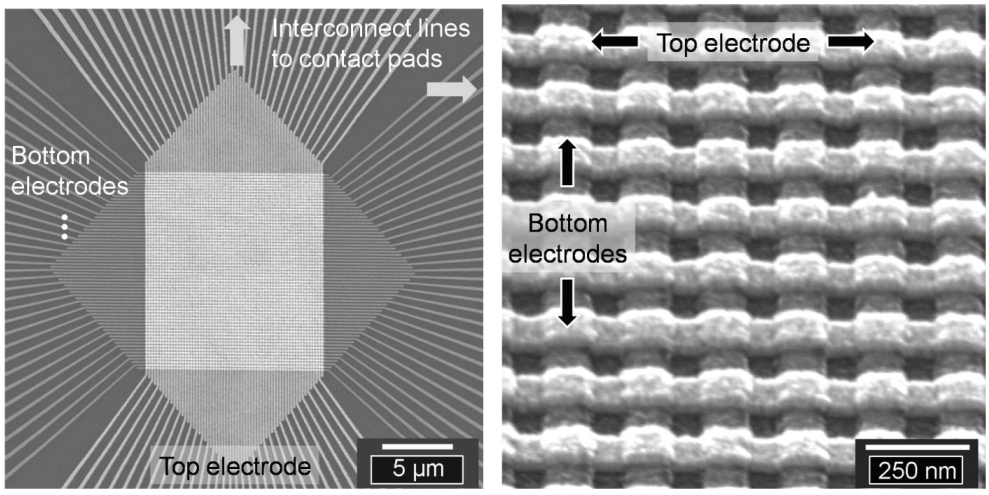
Figure 5.13: Resistance values for 200 nm wide nano word devices analogous to figure 5.12 with (a) 8 bit, (b) 16 bit and (c) 32 bit memory size.

outer than for the inner junctions. The periodical decrease of three resistances is related to the arrangement of the contact pads in a row-of-three. As the spare space for smaller devices was not used for a widening of the supply wires, all word structures yield comparable resistances ranging between approximately 7.5 kΩ and 8.5 kΩ for 100 nm half-pitch and between 6 kΩ and 7 kΩ for 200 nm half-pitch. The insulation between the metallization lines was excellent, and the insulation resistance on the SiO_2 substrate was extremely high and not measurable within the range of ±5 V.

5.4.3 Nano crossbar arrays

Nano crossbar arrays are the targeted core device for the integration of resistively switching thin films. In future applications, they might be coupled directly to control modules. Here, they are fabricated as templates with supply lines that comply with the ones presented for the word structures.

Figure 5.14 (a) shows a SEM picture of an array with a size of 64 × 64 bit, e.g. 4096 bit and a half-pitch of 100 nm resulting in a cell size of 0.04 µm². This is a storage density of 2.5 Gbit · cm^{-2}, which is comparable to 2.47 Gbit · cm^{-2} of NAND-flash memory in the 2007 roadmap [29]. Additionally, devices with storage sizes of $n \times n$ bit with $n = 8$, 16, and 32 were available. Furthermore, more robust arrays with 200 nm half-pitch but the same cell numbers were fabricated. SEM examinations, like figure 5.14 (b), and electrical continuity and crosstalk investigations of the lines showed a high functionality. This was done by 32 × 32 bit and smaller arrays that possessed end-to-end electrodes. Figure 5.15 (a) shows the resistance distribution of 32 addressed 100 nm wide bottom lines of a 32 × 32 bit array. Like for the word structure, the resistance pattern maps the design of the complete electrode and supply lines. The average resistance is below 9 kΩ, but due to the space needed by the crossing set of electrodes, the nano electrodes are 6.4 µm longer than those in the word structure. However, this increase was of less consequence because of the high fractional resistance of the used wedge-shaped interconnect line. Compared with figure 5.12 (c), the total resistance increased for nearly 1 kΩ.

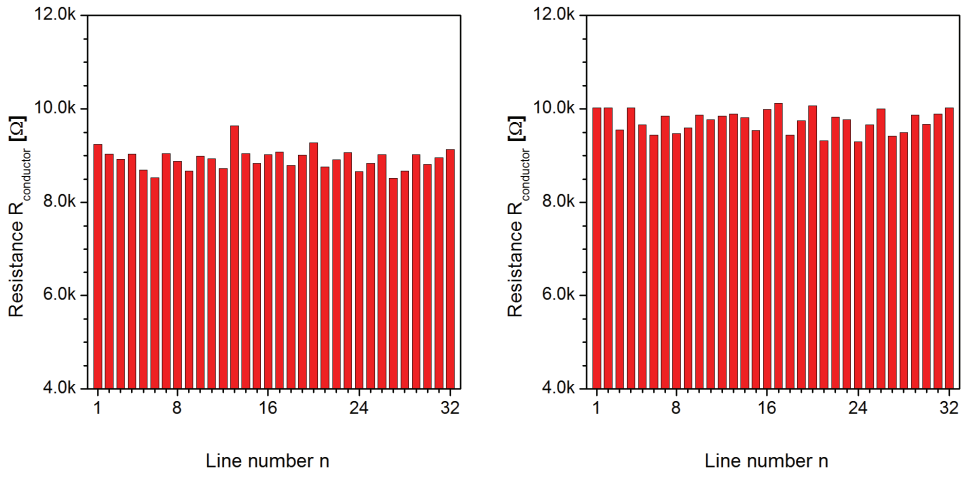


(a) (b)

Figure 5.14: (a) SEM top view of a 64 × 64 bit nano crossbar array with 100 nm wire pitch and 30 nm metal thickness. (b) Shows a detailed side view of the array with the course of the top electrode.

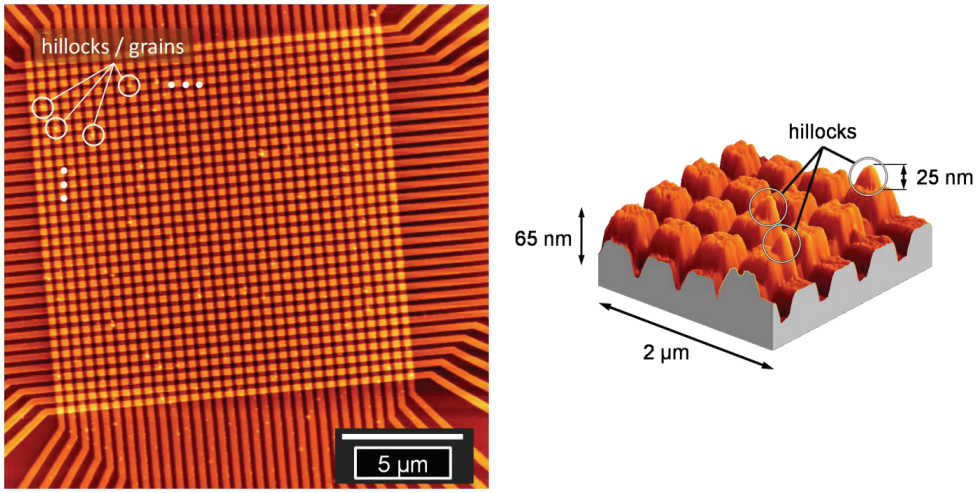
Figure 5.15 (b) shows the corresponding resistance distribution for a set of 32 top electrodes. Their layout is comparable to the bottom electrodes, but the determined resistances showed slight deviations and a comparably small resistance increase. However, the smooth covering characteristics of the reactively sputtered TiO_2 along the bottom electrode edges created defect free top electrodes, as shown in figure 5.14 (b).

Within this series several hundred 100 nm wide bottom electrodes were examined with only a few defective metal lines, resulting in a yield of 95%. The origin of the defects were mostly disturbances like dust particles interrupting the metallization layer. This is certainly a general



(a) (b)

Figure 5.15: (a) Conductor resistances for a 32 bit array with 100 nm wide conductors on SiO_2. (b) Electrode resistances of a nano crossbar array on top of 30 nm thin bottom electrodes covered by a 30 nm thin TiO_2 film.



(a) (b)

Figure 5.16: (a) AFM-scan showing randomly distributed impurities along the top electrodes in form of small particles. (b) Detailed 3-dimensional presentation showing impurities at the edges of the top electrodes.

practical issue related to the infrastructure and not to the lift-off process itself. The appearance of particles, which is normally related to lift-off processes, was very low for the Ti/Pt metallization. Therefore, 200 nm lines had a yield of nearly 100%.

The 100 nm wide top electrodes showed a yield of more than 60% due to the appearance of inhomogeneities as determined by AFM measurements such as in figure 5.16. These emerged from larger grains within the bottom electrodes that increased further during the TiO_2 deposition. Their height was about 20 to 30 nm as illustrated in figure 5.16 (b), and their diameter was in the range of nearly 100 nm. Therefore, this effect influenced the yield of 100 nm wide lines stronger than that of 200 nm lines, which was above 90%. Additional examinations of pure TiO_2 thin films as well as of pure Pt bottom electrodes confirmed the occurrence of these grains for the combination of the functional layer and the electrodes. But because of the redundant design of the word and array structures with the double-sided supply lines, the yield concerning the addressability of the precise junctions is essentially higher.

In conclusion, the fabricated devices present a reliable template for a multitude of investigations in connection with passive resistive switching architectures.

5.5 Nano metal line robustness

To examine the robustness of the fabricated structures, crossbar arrays with a wire width of 200 nm were stressed with a current of 1 mA. The investigated structures were common top electrodes on a thin TiO_2 thin film covering a set of 32 bottom electrodes. During a preliminary

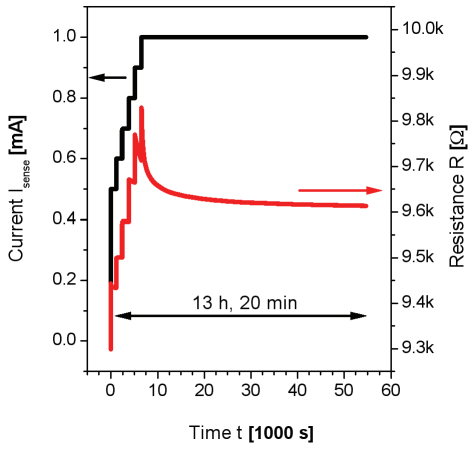


Figure 5.17: Long-term current load for a 100 nm wide top electrode. The current was increased step-wise to 1 mA and then sustained for more than 12 h.

test the electrodes were checked in respect of their functionality. Then, wires that showed no failure were used for a short-term test and stressed for 1 h with 1 mA. No devices showed any destruction or degradation. In a next step the medium-term endurance was tested. Therefore, top electrodes of 100 nm width of a 32 bit array were tested.

Figure 5.17 shows exemplarily the resistance characteristic of a long-term examination. A short sweep increased the current up to 500 µA where it remained for 20 minutes. Afterwards, the current was increased by steps of 100 µA up to 1 mA, intermitted by constant periods of 20 min to detect an early destruction. Finally, the sample was strained for more than 12 h. The wires showed neither destruction nor a considerable degradation. However, the resistance decreased irreversibly for several hundred Ω. The origin of this effect was not examined, but an annealing of the metal lines at elevated temperatures, caused by the high current density, can serve as explanation.

Finally, 200 nm and 100 nm wide top electrodes showed a high robustness strained by currents of 1 mA for several hours, which was more than sufficient for switching experiments.

5.6 Insulation characteristics of nano metal lines

In general, the insulation resistance between adjacent nano metal lines on a SiO_2 surface was higher than the input resistance of the measuring amplifier and from there not determinable. As a result, the sample substrate did not influence the static electrical characteristics of the presented devices.

In the following, the static crosstalk of neighboring wires, caused by the 30 nm thin reactively sputtered TiO_2, will be considered. Figure 5.18 exemplifies the $R(V)$ characteristic of two neighboring Pt bottom electrodes in a 32 bit array with 100 nm conductor width. The pitch between both lines in the center was 100 nm. It broadened up continuously along the supply lines. A TiO_2 layer covered the set of electrodes with a variable electrically effective thickness, caused by the uneven covering of the metal structure. Thus, the set of electrodes evaded from a

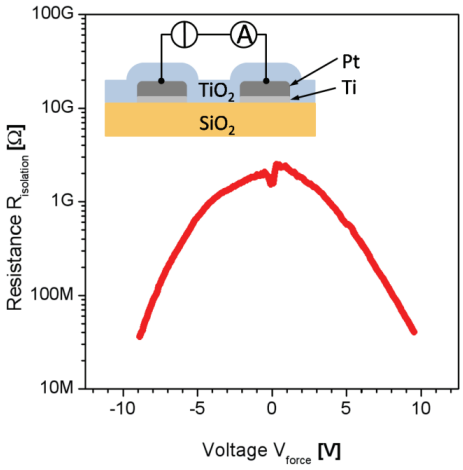


Figure 5.18: Insulation resistance exemplified for two adjacent conductors covered with TiO_2.

simple geometrical description, which was enforced by the large and variable length of the central wires. On this basis, the examination shows the insulation properties and ability to suppress resistance switching between two adjacent metal lines. A geometrical dependency or material analysis was not the target of this investigation. The *R(V)* behavior shows a symmetrical resistance decrease, starting above 1 GΩ for small voltages and reaching several 10 MΩ within a voltage range between ±8 V and ±10 V. However, the TiO_2 film showed a stable behavior and no tendency for electroforming or resistance switching between neighboring bottom electrodes up to voltages of 10 V.

The same experiments were performed for a set of 32 electrodes applied on top of a 30 nm thin TiO_2 film building a Pt/Ti/TiO_2 stack on a SiO_2 substrate. The layout of these metallization lines was equivalent to the above mentioned pattern. Figure 5.19 shows the *R(V)* characteristics of this setup with resistances in the range of several ten GΩ. However, up to 10 V and

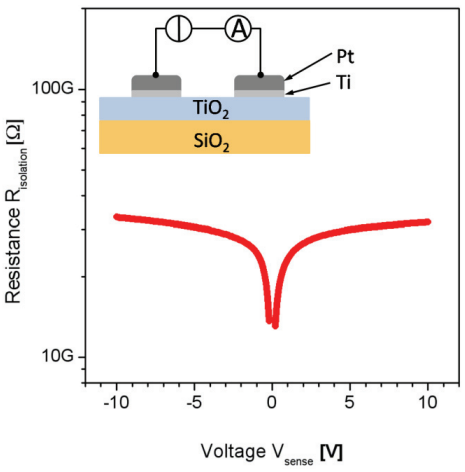


Figure 5.19: Insulation resistance of two adjacent top electrodes of a 32 bit nano crossbar array with 100 nm wire width and 100 nm wire pitch. The structure does not include a bottom electrode.

higher, no resistance degradation or resistance switching was observed, which could impact the functionality of an array.

The difference between the nature of the top electrodes and the bottom electrodes could be explained by the different interface of Pt/TiO_2 and Ti/TiO_2 and the difference concerning the deposition methods of sputtering and thermal evaporation. The Pt/TiO_2 interface generates a Schottky-barrier between a metal and a weak n-type semiconductor, here the TiO_2 in the unformed state. The exponential current response, which was measured for the $R(V)$-curve in figure 5.18, confirms this. However, the Ti/TiO_2 interface shows a rather ohmic characteristic, which is presented figure 5.19. The difference between the resistance ranges of both setups is explained by the deposition technique of the TiO_2 and Ti/Pt electrode. In the first case, the contact resistance might be lower, because of the high kinetic energy of the sputtering process in comparison with the low energetic evaporation of the metallization lines. Additionally, the interface area is essentially larger for the bottom electrodes, since they were covered on three sides. Finally, the morphology of the TiO_2 on patterned Pt electrodes might be different in comparison with layers on the plane SiO_2 substrate.

In summary, adjacent electrodes with a length of more than 10 µm and a distance of only 100 nm were very well insulated against each other; a fact that emphasizes the technological quality of these devices. In combination with TiO_2, the resistance showed a nonlinear behavior with a strong decrease around 10 V, which is, however, higher than any control signal for the operation of single cells. As a result, switching directly between neighboring metal lines was not detected and appears to be electrically unattractive for 100 nm large gaps and voltages below 10 V.

The next step of the electrical tests was related to the insulation resistances of adjacent metal lines within each electrode level of a complete array with top and bottom electrodes. Figure 5.20

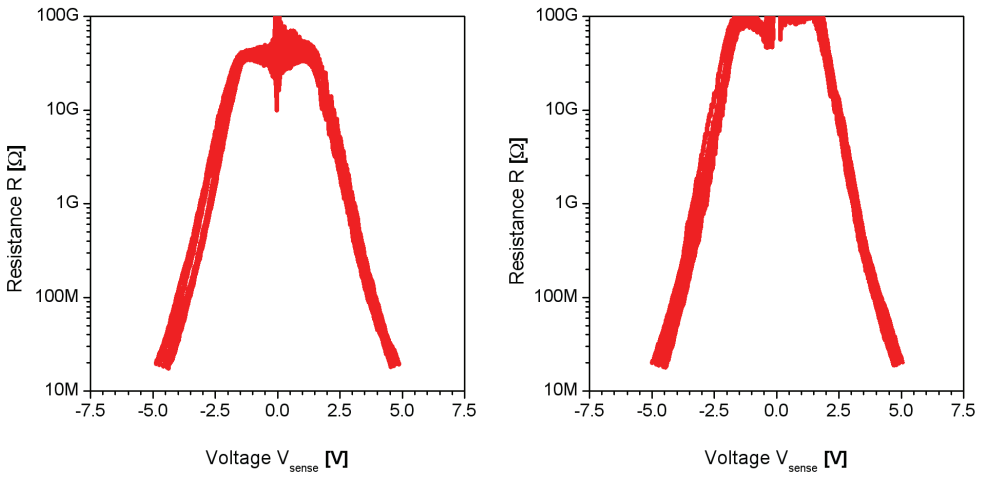


Figure 5.20: Initial resistance between two neighboring electrodes (a) for the bottom electrodes and (b) the top electrodes. Shown are all seven curves for both levels, each.

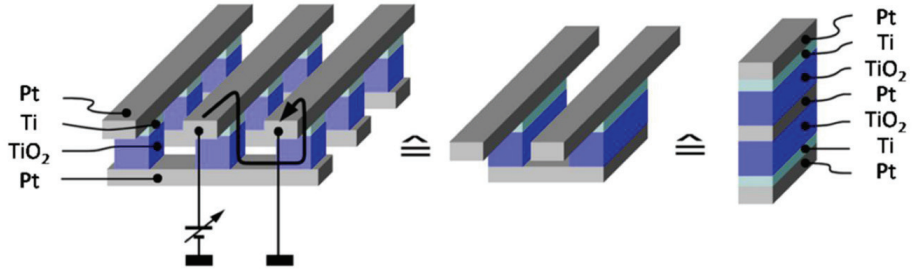
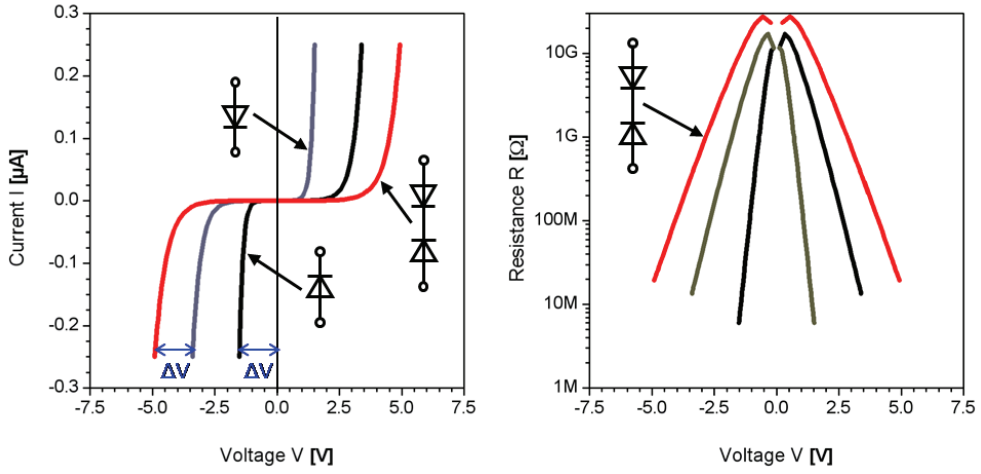


Figure 5.21: Illustration of the current flow for the explanation of the crosstalk in adjacent nano wires due to opposite diode-like devices. The left figure is a section of a crossbar array that is unified to the relevant stack shown on the right side.

presents the corresponding $R(V)$ characteristics of an 8 bit crossbar array with 200 nm metallization lines. The voltage signal was applied between two adjacent electrodes of the same level. The curves are symmetric with a cut-off region between -1.5 V and 1.5 V and a comparatively slight difference in resistance of 40 GΩ for the bottom and 90 GΩ for the top level. This difference was caused by different leakage currents directly between the electrodes of the considered level.

For higher voltage values, the resistance decreases for about three orders of magnitude to several 10 MΩ at ±5 V. The reason for this is found in the weak rectifier characteristic of the single junctions with the Pt/TiO_2/Ti/Pt stack. The potential difference between two metal lines drops over the TiO_2 between the metal of the same level, but creates also a voltage divider over the junctions and the metal wires of the opposite level. The latter is shown in figure 5.21. For an



(a) (b)

Figure 5.22: (a) Model calculation by an exponential $I(V)$ fit for a single junction. The black curve corresponds to the typical initial $I(V)$ characteristic of a Pt/TiO_2/Ti/Pt stack, whereas the grey curve illustrates the response of an inverted stack. The red curve is the combination of both rectifiers connected against each other. (b) The red $R(V)$ curve shows the corresponding nature of the insulation resistance between two adjacent wires.

$n \times n$ array, n of these paths are in a parallel connection and can be merged. Finally, the counter electrode creates a negligible resistance but a relevant interface, which results in a Pt/Ti/TiO_2/Pt/TiO_2/Ti/Pt stack. This is the combination of two junctions in series that are directed against each other and consequently build two counteracting rectifiers. The electrical nature corresponds well with this model as shown in figure 5.22. Two exponential fits were used to describe the current response of a single junction. One of these junctions was in forward direction, here illustrated by the grey curve, and the other in reverse direction, illustrated by the black curve. A serial connection of both resulted in the expansion of the total current with $I(V\text{-}\Delta V)$. The resulting $R(V)$ curve is illustrated in red in figure 5.22 (b) and fits well with the measured curves in figure 5.20.

That property of the nano crossbar array with TiO_2 shows that parasitic current paths between the electrodes appeared only in the small voltage range where the rectifier of the junction blocks the current. The involved values were however too low to provoke an electroforming within an electrode level, which agrees well with the above described examinations. Caused by the nonlinearity of the junctions, a current flow emerged prior through the corresponding cross point as their conductance prevailed the parasitic path. This applies for bottom and top electrodes.

On this basis, intrinsic bypasses inside the TiO_2 film did not seem to play a role to an extent that influences the functionality of the switching devices.

6 Investigations of resistance switching in TiO_2

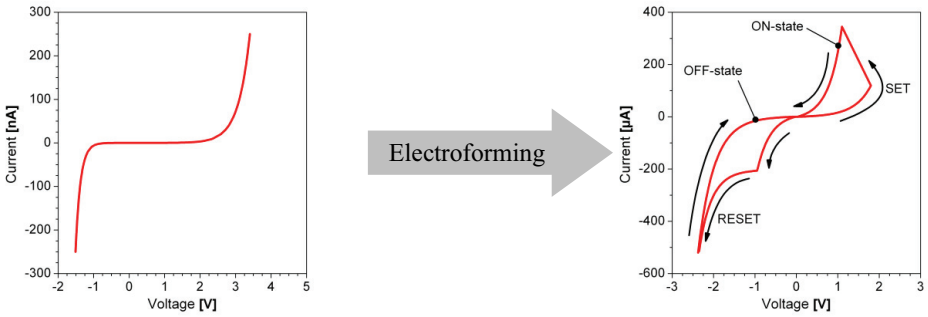
The first analysis of resistively switching TiO_2 integrated into crosspoint junctions were performed at structures with lateral sizes in the micrometer range. Test devices that are similar to planar 2-dimensional capacitors with a metal/insulator/metal stack were examined previously by Jeong [111]. However, these did not provide an asymmetrical material combination in regard to the Pt/Ti electrodes and are therefore not comparable in detail. The observed switching performance was nevertheless very promising for an integration into crossbar architecture and a further size reduction. The additionally incorporated Ti was considered to support the switching mechanism by a nearly ohmic interface.

To estimate the downscaling potential step by step, micrometer sized devices served as an intermediate control level leading to the examination of nano sized structures. Due to the comparably lower effort of optical lithography for micro devices in contrast to electron beam direct writing for nano devices, switching parameters and probably occurring challenges could be examined more efficiently in advance.

The following chapter explains the essential electroforming process in consideration of the polarity and controlled signal. Then, the used micrometer sized functional devices are described before their quasi-static switching characteristics with ALD or reactively sputtered TiO_2 is presented. This chapter closes with the electrical characterization of nano sized junctions with a special consideration of the scaling potential.

6.1 Electroforming of TiO_2

The electroforming process is the transfer from the initial state to the switching state, as illustrated in figure 6.1. This conversion needed a nonreversible and special onetime operation. As the inert transaction during this process was still unclear, no distinctly ideal method was found. Four approaches were therefore accomplished and are presented and discussed in the following. However, all methods resulted in stable conditions concerning reversible switching. In general, the electroforming can be performed voltage or current controlled providing an amplitude to changes the electrical property of the TiO_2 film. The simplest way is the application of a constant voltage or current that forms the device after some time. However, the reported time frames were partially very long [58]. Even though the forming time depended on the magnitude of the applied signal, deviations made it hard to estimate a reliable set of parameters. On the one hand, it was possible that no electroforming commenced if the amplitude was too low. On the other hand, a direct transfer into a permanent LRS could occur if the amplitude was too high. The recurring search for appropriate parameters made this method unsuitable for experimental applications with a large number of structures. Sweeping signals with constantly increasing amplitudes showed however satisfying results. The rising voltage or current passed in



(a) (b)

Figure 6.1: (a) Scheme of an initial current response of a junction with TiO_2. (b) After the electroforming, the junction has essentially lower resistances and is switchable. Note the difference of three orders of magnitude for the current response.

this way through any predefined interval and covered a certain range of deviations of forming parameters

Due to the asymmetry and the slightly rectifying nature of the Pt/TiO_2/Ti/Pt stack, it was necessary to examine both polarities. In principal, all voltage signals were applied at the top electrode with the Ti/TiO_2 interface, which applies for all presented measurements in this study. The initial characteristic of a test device, which was used for the following electroforming evaluation, is presented in figure 6.2. A negative voltage applied at the top electrode operates the device in forward direction. The cut-off voltage for the positive polarity amounted to around 1 V. Two effects served as explanations for the asymmetry: The TiO_2 contains n-type semiconducting fractions that create a Schottky-barrier in combination with the Pt and a more ohmic interface with the Ti/Pt electrode. Additionally, the effect of the deposition method is unclear. The top electrode was deposited by thermal evaporation with a low energetic impact, whereas the bottom electrode was exposed to a high energetic impact during the TiO_2-sputtering. Such a high energetic ion bombardment might deteriorate the lower TiO_2/Pt interface.

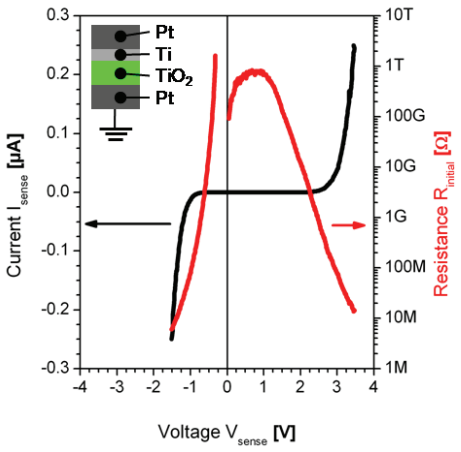


Figure 6.2: Initial $I(V)$- and $R(V)$-characteristic of a crosspoint junction with different top and bottom electrode materials.

6.1.1 Voltage controlled electroforming

Electroforming with a positive voltage sweep

The first approach was the electroforming by a positive voltage sweep. The signal was applied to the top electrode (Pt/Ti/TiO_2), whereas the bottom electrode (TiO_2/Pt) was grounded. Experience indicated that a low slew rate of the electroforming signal yielded marginal failures. So, first investigations with approximately 5 mV · s^{-1} provided a reliable electroforming. In contrast, high slew rates, in the range of 1 V · s^{-1}, ended often in very low and non-switchable resistance states. Any kinds of reset-process led to the destruction of interconnect wires by overheating and melting of the metal.

Experience showed that an external current limit was required. This prevented a destructive dielectric breakdown of the TiO_2 layer. Additionally, it was reported that unipolar and bipolar switching modes could be adjusted by the maximum forming current [111]. However, a reasonable value for the maximum current had to be defined taking two demands into account: First, the junction had to pass the electroforming step before it reached the limit. Second, the therewith associated power dissipation had to be small to avoid a thermal destruction. In the electroforming step demonstrated in figure 6.3 (a) a current limit of 50 µA was predefined.

For small voltages the current response followed the rectifying nature of the Pt/TiO_2/Ti/Pt stack in reverse direction. Above 2 V the conductivity of the material increased exponentially, and the current response started to oscillate between 4 V and 5 V. Finally, the resistance decreased abruptly above 5 V and 18 µA for more than two orders of magnitude. The finally received condition was a very low LRS between 1 kΩ and 2 kΩ, which is shown in figure 6.3 (b). The total difference in comparison with the initial state amounted to seven orders

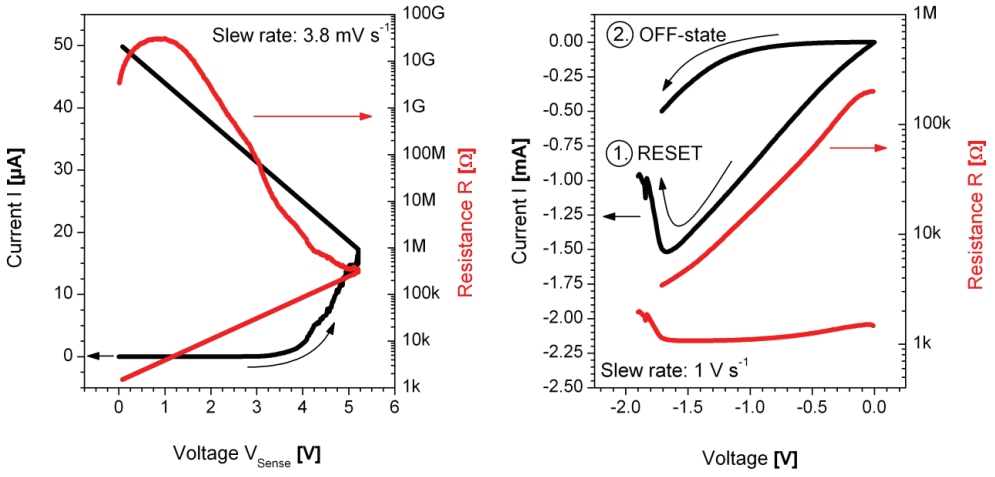


Figure 6.3: (a) Measured electroforming process with a positive voltage sweep. (b) *I*(*V*) and *R*(*V*) characteristics of the reset-behavior and the resulting HRS state.

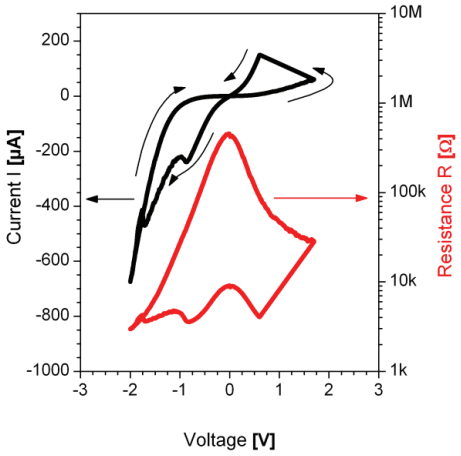


Figure 6.4: Determined resistive switching characteristic of the current response (upper curve) and resistance (lower curve) of a junction formed by a positive voltage (see figure 6.2).

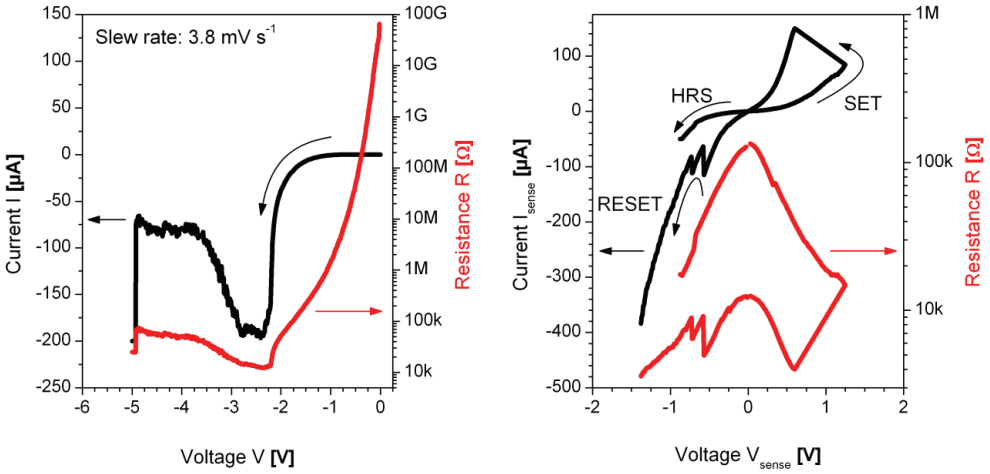
of magnitude. This could be reset by a negative voltage sweep with 1 $V \cdot s^{-1}$, which is essentially faster than the forming sweep. The reset itself was indicated by an increase of the resistance below -1.7 V, which led to the HRS with 200 kΩ for small voltages. At this point the electroforming process was completed and the junction stabilized its LRS around 9 kΩ within the next three cycles.

The resulting $I(V)$ and $R(V)$ characteristics of this device are demonstrated in figure 6.4. Here, a current limit of 150 µA for the positive polarity and maximum negative voltage amplitude of -2 V protected the device from overcharge. The comparison of the reset-voltage in figure 6.3 (b) with the one in figure 6.4 indicates a difference of nearly 1 V. Thus, it was unclear whether the first reset-sweep belonged to the electroforming process or if it was a result of it.

In summary, an adequate adjustment of the current limit was an issue in regard to occurring deviations. In spite of small current limits, devices were often unfeasible. Additionally, the tendency of an inverse switching direction or the interference of two switching effects leading to the combination of a set- and a reset-process within one polarity was sometimes observed during subsequent cycles.

Electroforming with a negative voltage sweep

Due to the asymmetrical design of the material stack it was a general question, whether both polarities could be used for the electroforming. The slightly rectifying nature promised furthermore a different set of parameters if this method would be applicable. So, a negative voltage sweep with a comparable slew rate was applied to transfer the TiO_2 into the resistive switching state. Similar to the positive voltage driven electroforming, a current limit needed to be set to an appropriate value. Here, 200 µA satisfied the demands for the device whose examined forming is presented in figure 6.5 (a). It is worth to mention that all presented electroforming characteristics within this section were recorded with comparable devices in regard of composition and dimensions.



(a) (b)

Figure 6.5: (a) Electroforming with a negative voltage sweep and a current limit of -200 µA. (b) First set- and reset-sweep after the electroforming process.

For small voltages the combination of a TiO_2/Ti thin film with Pt electrodes continues the $I(V)$-characteristic of the initial state in forward direction for the negative polarity. Between 0 and -1 V the resistance decreased over five orders of magnitude. A small but sharp bend ended this decrease and marked the beginning of a resistance increase for several ten kΩ which was interfered with oscillations. The device was formed subsequently by a small and abrupt resistance degradation. Then, the process was stopped when the current reached its predefined limit. Figure 6.5 (b) exhibits a resistance above 100 kΩ for small voltages, which refers to a common OFF-state. A faster quasi-static voltage sweep (slew rate: $1V \cdot s^{-1}$) with positive polarity switched the device into the ON-state. Subsequently, a negative voltage sweep was used to reset the junction. The comparison of figure 6.5 (b) with the stable switching curve in

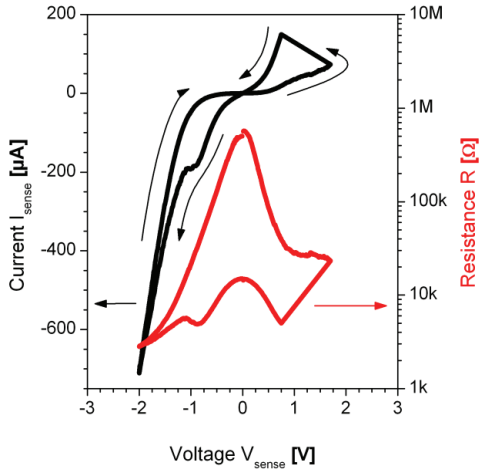


Figure 6.6: Resistance switching of a junction that was electroformed by a negative voltage sweep.

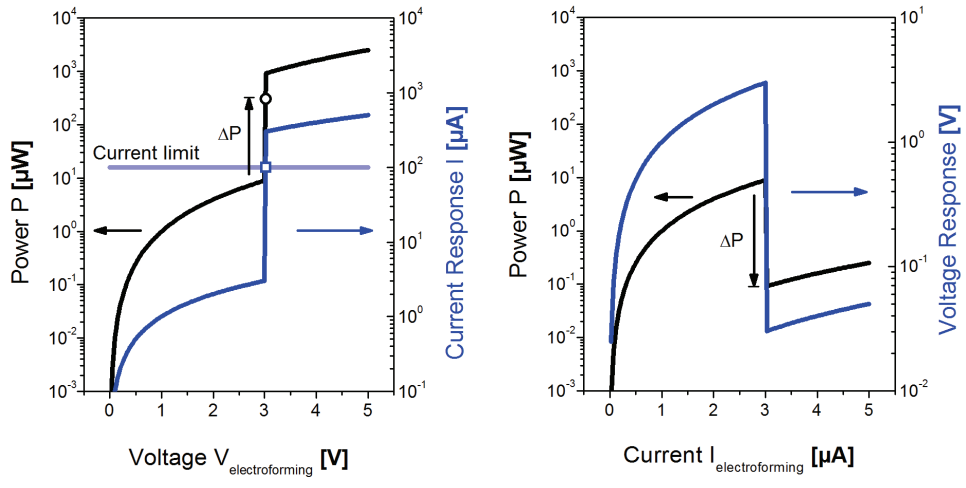
figure 6.6 yielded comparable parameters that suggested a termination of the electroforming after the initial voltage sweep.

Anticipating later results, the electroforming was subject to the junction area and to variations of parameters such as forming voltages and currents. Thus, it was difficult again to define an adequate current limit. In addition, experiments indicated that the electroforming step was time dependent. Voltage sweeps with a high slew rate needed also higher forming currents resulting, in turn, in an increased breakdown probability. However, the responding currents were generally higher for the negative polarity and the determined threshold voltages were nearly equal.

In summary, voltage controlled electroforming worked properly if the current limit was reasonably adjusted. The latter was nevertheless an issue with respect to deviations within a series of devices. Additionally, the positive voltage sweep created a very low LRS with a nearly constant $R(V)$-characteristic. It is unclear whether this was a low bipolar switchable or a steady ON-state, because the reset-signal overloaded the supply electrodes and destroyed the device.

6.1.2 Current controlled electroforming

These uncertainties lead to the contemplation of a current controlled treatment. In this case, no current limit was necessary, which is explained by the following example. An abrupt resistance degradation for more than one order of magnitude was assumed at a threshold voltage of $U_{e\text{-}form} =$ 3 V. For simplification, the initial and the formed resistances were constant with 1 MΩ and 10 kΩ in both cases. The voltage $U_{e\text{-}from}$ or current $I_{e\text{-}form}$ is nearly constant around the forming point of the current or voltage controlled electroforming, whereas the resistance



(a) (b)

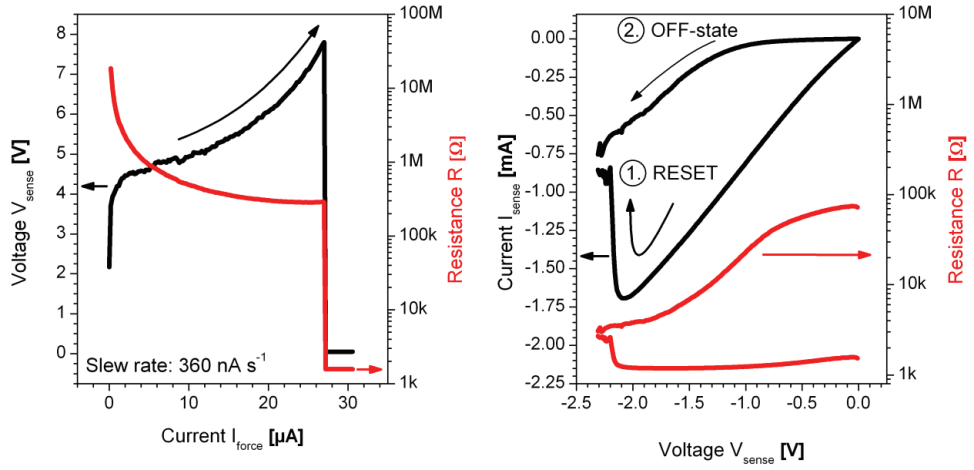
Figure 6.7: Schematic diagram of a voltage controlled (a) and a current controlled (b) electroforming process. The applied signal is sweeping from zero to the maximum amplitude. The responding signal is indicated with the blue curve and the power dissipation is given as the black curve.

decreases for $\Delta R = 990\ k\Omega$. As an example for the voltage controlled electroforming figure 6.7 (a) shows that the corresponding current increases with $\Delta I_{e\text{-}form} \approx U_{e\text{-}form} / \Delta R$. Following, the power dissipation $P = U \cdot I$ increases with $\Delta P_{e\text{-}form} = U_{e\text{-}from}^2 / \Delta R$ inversely proportional with ΔR. To protect the device from thermal breakdown due to Joule heating, an active current limit has to be used that reduces the voltage rapidly to keep the current under a certain limit. The current controlled electroforming is demonstrated in figure 6.7 (b) and results in a voltage decrease at the forming step of $\Delta U_{e\text{-}form} \approx I_{e\text{-}form} \cdot \Delta R$ proportional to the decrease of ΔR. This is in conjunction with the decrease of the power dissipation $\Delta P_{e\text{-}form} = I_{e\text{-}from}^2 \cdot \Delta R$ and needs no additional limit. The advantage is that the power dissipation within the device is always lower than for the voltage controlled electroforming. Additionally, the predefined current range for the electroforming can be large enough to provide a certain electroforming.

Electroforming with a positive current sweep

The electroforming by applying a positive current sweep seizes the previously mentioned advantage. The choice of a reasonable slew rate for the current is comparable with the above mentioned case for voltage sweeps. Fast sweeps resulted in higher currents at the forming peak and involved higher defect probabilities. Satisfying results were obtained with slew rates between 100 and 500 nA · s^{-1}. So, figure 6.8 (a) exemplifies the electrical characteristic for about 360 nA · s^{-1}. Due to the cut-off region for the positive polarity, the voltage increased essentially for lower currents. The exponential trace of the current response was interfered with a distinct noise. In the range of several ten µA and several V the material is formed and the resistance drops from several hundred kΩ down to some kΩ.

A subsequent examination evidenced an electroforming into the LRS. The first negative reset-sweep switched the junction back into the HRS, which is demonstrated in figure 6.8 (b).



(a) (b)

Figure 6.8: (a) Electroforming of a crosspoint junction by a current sweep with positive polarity. (b) First reset voltage sweep that switches the cell into the OFF state.

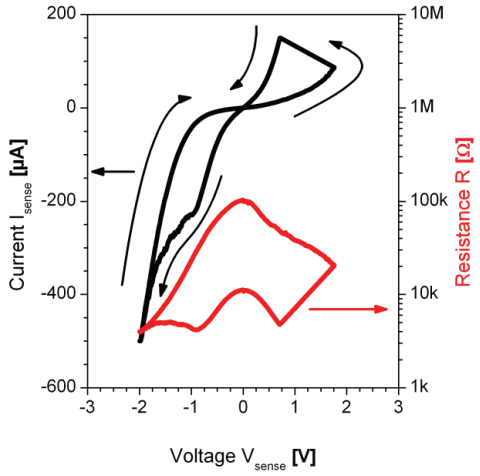


Figure 6.9: Resistance switching of a junction that was formed by a positive current.

The therefore needed current was in the mA range because of the low LRS, which was a general property of an electroforming process with a positive polarity. Also the qualitative course of the $V(I)$ characteristic is comparable to the $I(V)$ characteristic in figure 6.3, even so the obtained values for current and voltage were higher.

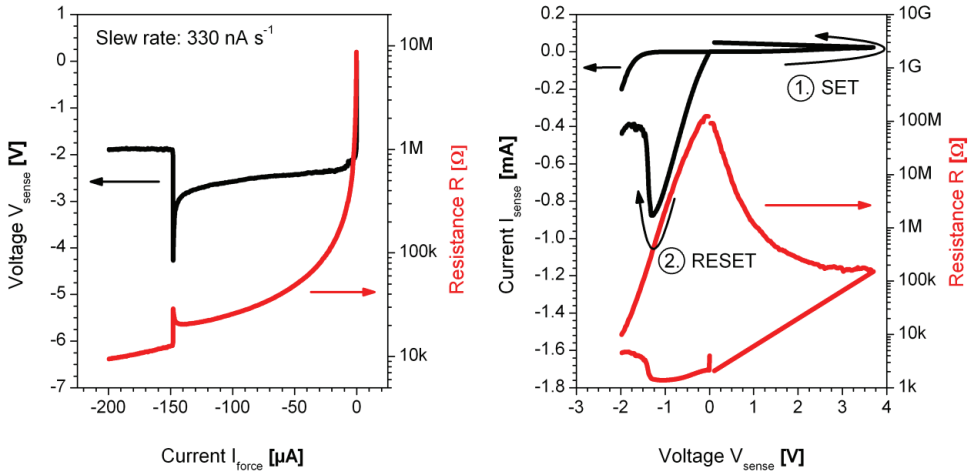
However, the switching characteristics that are demonstrated in figure 6.9 featured the expected nature. Nevertheless, the positive polarity that forms into an ON-state resulted often in a low LRS, which could not be reset without destroying the supply lines of some devices.

Electroforming with a negative current sweep

To combine the advantage of a current controlled electroforming with the advantage of a transfer into the OFF-state, a negative current sweep is used. The signal as well as the voltage response is demonstrated in figure 6.10 (a).

Comparable with the positive sweep the method showed good results for a slew rate of around 330 nA · s^{-1}. The voltage response indicated no noise in comparison to the other tested methods, but seemed to increase asymptotically and later exponentially before the device electroformed abruptly. The resistance decreased finally to about 10 kΩ. This value belonged to the HRS, which is however very low due to the nonlinearity of the material.

As shown in figure 6.10 (b), a fast positive quasi-static voltage sweep switched the device into the ON-state. The current limit for this set signal was commonly between 50 and 150 µA. A subsequent negative sweep with a minimal amplitude of -2 V reset the resistance state. Figure 6.11 shows the stabilized switching signal after 10 cycles. Compared with the first set- and reset-response after the electroforming, the OFF-resistance was about two orders of magnitude lower than during the repeated switching. The exceptional high set-voltage was typical for the first transfer from the formed OFF-state to the ON-state. Also, the resistance of the first ON-state was nearly one order of magnitude lower than the stabilized ON- resistance



(a) (b)

Figure 6.10: (a) Electroforming sequence characterized by a negative current sweep. (b) Characteristic features of the first set- and reset-sweep. Both were performed voltage controlled.

that results in a correspondingly high reset-current. The switching parameters stabilize within the first two or three sweep cycles to values comparable with the ones in figure 6.10. As the first switching cycle differed considerably from the subsequent switching cycles in regard of the gained parameters, it was questionable whether it was part of the electroforming or already finished after the current sweep, above all, as the nature is completely comparable.

The negative current sweep worked well for all subsequently tested devices. The sweep itself led to the forming points of the functional devices regardless of deviations and needed no limits. In addition, most devices were transferred into the OFF-state.

The difference between a current and voltage driven electroforming correspond to technical aspects, but the processes are physically completely comparable. However, the used polarity

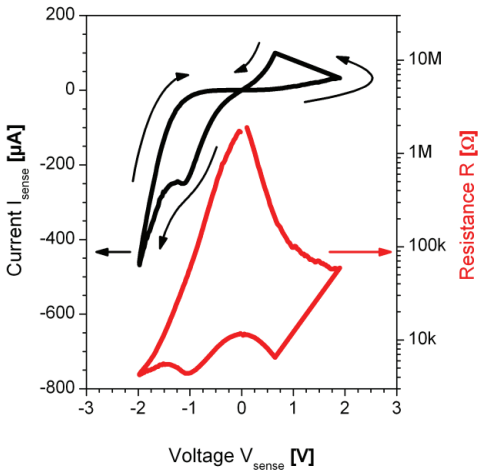
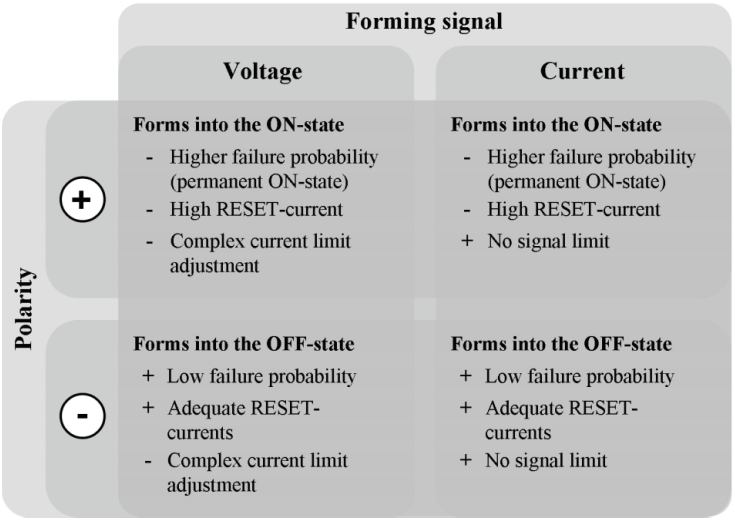


Figure 6.11: Stabilized electrical characteristic, $I(V)$ and $R(V)$, of the device that was electroformed by the negative current sweep.

affects the characteristic of the device accordingly to the model of the oxygen vacancy distribution. The generation of vacancies during the electroforming seems to be independent of the polarity, because the transfer into a switchable state occurs in both cases. However, the resulting state (HRS or LRS) depends on the applied polarity. For a positive signal, all created vacancies are shifted towards the TiO_2/Pt interface and reduce there the Schottky barrier width. As a result, the system electroform into the LRS. For a negative signal, all vacancies drift towards the TiO_2/Ti interface and the opposed Schottky contact remains in its rectifying state. A second electroforming step with a different polarity, described by Jeong et al. [58], is not needed, because the TiO_2/Ti/Pt stack offers a nearly ohmic interface.

Consequently, all following devices were electroformed by a negative current sweep. For a better overview, the next chart summarizes the phenomenological features of the applied methods.



Even though the electroforming by a negative current showed the best properties within this study, it is important to note that all methods are suitable for the electroforming process. This provides an adaption for future applications, as precise demands of externally generated control signals are unknown today.

6.2 Design of micro test structures

Single isolated crosspoint junctions, as shown in figure 6.12, were built for the electrical characterization of TiO_2. The electrodes were thermally evaporated. Here, the micrometer wide bottom electrodes comprise a 5 nm thin Ti adhesion layer to promote a reliable adhesion of the electrode on the SiO_2 surface of the substrate. The actual conductors were made of a 50 nm thin

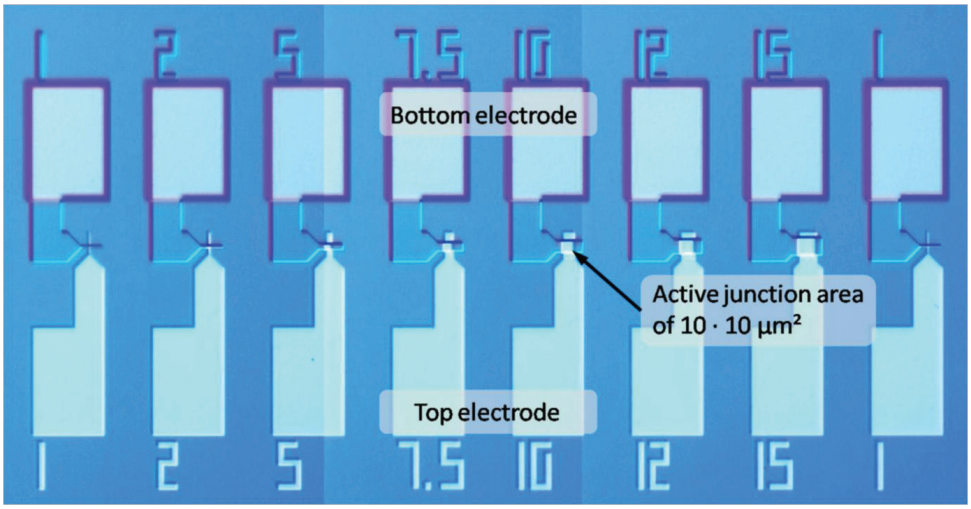


Figure 6.12: Single micro cross point junctions. The width of each electrode is given next to the contact pad in micrometer. The micrograph was taken by a polarization filter creating a three-dimensional illusion.

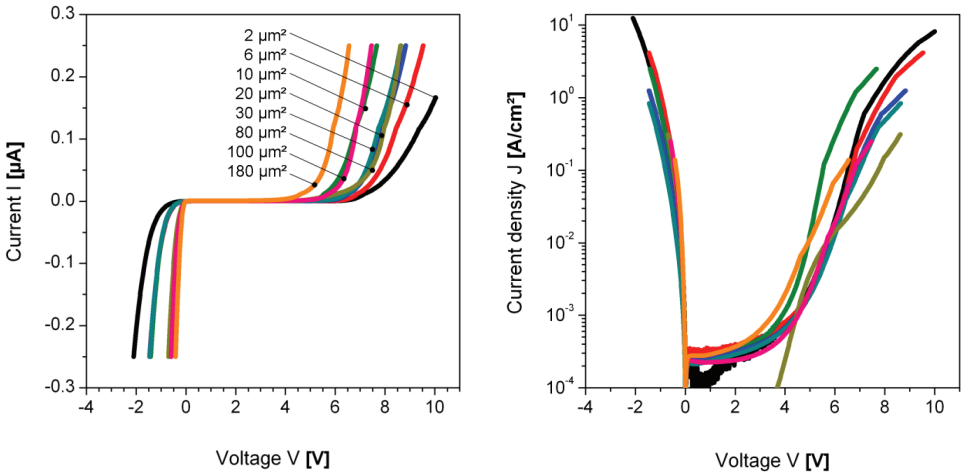
Pt layer. These were covered with a 50 nm thin TiO_2 layer fabricated by ALD or reactive sputtering. In contrast to the bottom electrodes, a 20 nm thin Ti layer was applied as top electrode, which was covered again by a 50 nm thin Pt layer. The insertions of the upper Ti layer had two reasons: Experiments revealed that TiO_2 is only reliable as substrate layer for sputtered Pt. So, appropriate adherence strength is not provided for thermally evaporated Pt, which requires therefore a pure Ti adhesion layer. Additionally, the Ti served as an asymmetric interface in comparison with the lower Pt interface. This asymmetry was expected to improve the switching properties in contrast to symmetric $Pt/TiO_2/Pt$ stacks, which gained the needed asymmetry by the directed electroforming step. A 20 nm thin layer should provide enough volume to generate a Ti/TiO_2 gradient that supports the switching.

The lateral size of the electrodes was in both cases between 1 µm and 15 µm, which resulted in a junction area between 1 µm² and 225 µm². Some examples are given in figure 6.12. As the width of the bottom and the top electrode was varied, not only squared junctions were fabricated but also rectangular formed structures ranging from 1 · 15 µm² to 15 · 1 µm².

6.3 Electrical characteristics of TiO_2 deposited by atomic layer deposition

The electrical characterization of the micro-crosspoints was performed by means of quasi-static signals. The parameters of the control signal have already been described in chapter 4. Nevertheless, it is important to mention again that the electrical signal was applied to the Pt top electrode that enclosed the Ti layer. The bottom electrode was accordingly grounded.

The initial state of the pristine TiO_2 deposited by ALD is presented in figure 6.13. The current response indicates the asymmetry by the electrode material. The negative part of the curve has a



(a) (b)

Figure 6.13: Initial state of an ALD-TiO_2 thin film. (a) Shown are the linear $I(V)$ characteristics for different junction areas and (b) the corresponding current densities in a semi-logarithmic plot.

very small cut-off voltage in the range of some mV. The cut-off voltage for the positive range amounts to several V. A tendency emerges for the forming current that increases with increasing junction size. As a corresponding result, the current density for several devices with different junction areas is in a comparable range, although a deviation superimposes the direct dependency between the current response and the related area. The scattering within the current density for positive voltages is essentially higher. A reason for any dispersion might be the multitude of inhomogeneities within the layer, the roughness of the electrode interfaces and, above all, disturbances along the edges of the bottom electrode.

Figure 6.13 (b) suggests the characteristic of a weak Schottky-barrier of the Pt/TiO_2 interface. Here, the curve is bended slightly, which might be the result of leakage currents and a serial path resistance arising from the ohmic part of the TiO_2/Ti interface. However, the measured curves reflected the initial asymmetry of the Pt/TiO_2/Ti/Pt stack and served as a first indicator for a fully functional device. To prevent any disadvantageous changes in the device, the initial $I(V)$ measurements were performed with a current limit, here 250 nA. In the case that this was too high, particularly for positive voltages, the current response changed irreversibly or the device sustained a breakdown in some cases.

Electroforming characteristics

A slow negative current sweep with an adapted slew rate of -10 $\mu A \cdot s^{-1}$ was a reliable method to electroform the micrometer large ALD devices. The corresponding voltage response is presented in figure 6.14 and indicates a dependency between junction area and forming current. Small areas needed by trend a small forming current, which was however superimposed by variations. Due to these deviations, it was once again not possible to examine the dependencies of the electroforming process. The cause was the abovementioned 3-dimensional setup of the thin film

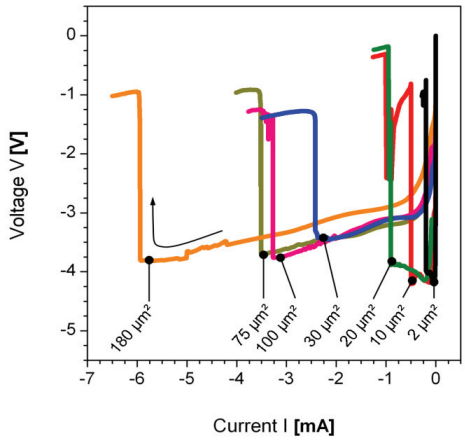


Figure 6.14: *V*(*I*) characteristics of the electroforming process by a negative current sweep for ALD-TiO_2 with different junction areas.

with the top electrode covering the bottom electrode and inhomogeneities of the film morphology. However, as the sweep travelled through a wide current range, these deviations could be intercepted. Also the corresponding time variations were within an acceptable scope, and electroforming could be succeeded reliably.

After the electroforming, the cells were in the OFF-state and needed to be switched on. This was done by a faster quasi-static positive voltage sweep with about 1 $V \cdot s^{-1}$. The slew rate corresponded to those that were used for the general quasi-static analysis of the switching. The risk of a hard breakdown during the first set had to be prevented by a tentative current limit, which was therefore set to small values, e.g. 100 – 500 µA. This restriction was important due to the fact that significantly higher current limits resulted often in very low and nearly linear ON-resistances. Those were comparable with the stable ON-states reached by an electroforming with a positive signal, and a destruction of the device during the reset-sweep was often the consequence. Figure 6.15 exemplifies such a breakdown and suggests an overheating of the supply line during the reset-step caused by extremely high reset-currents over 10 mA.

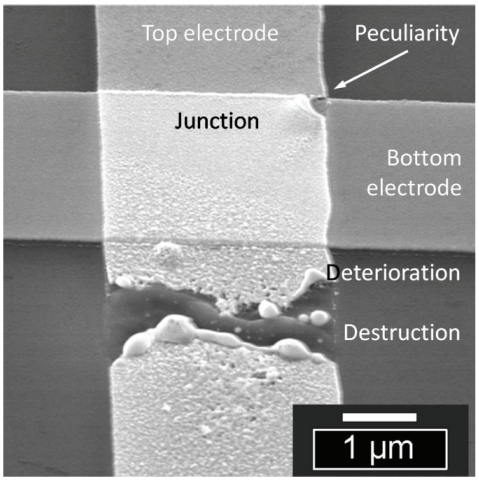


Figure 6.15: Destructed electrode caused by a high reset-current after a fast electroforming process.

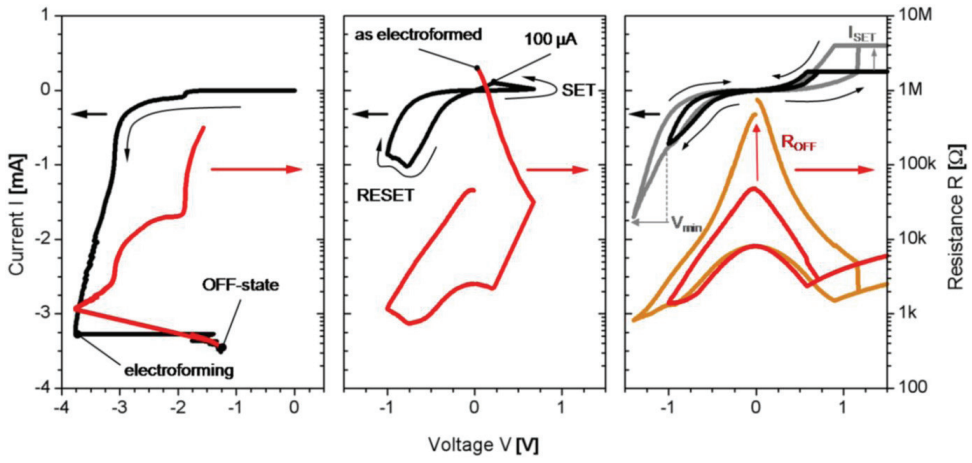


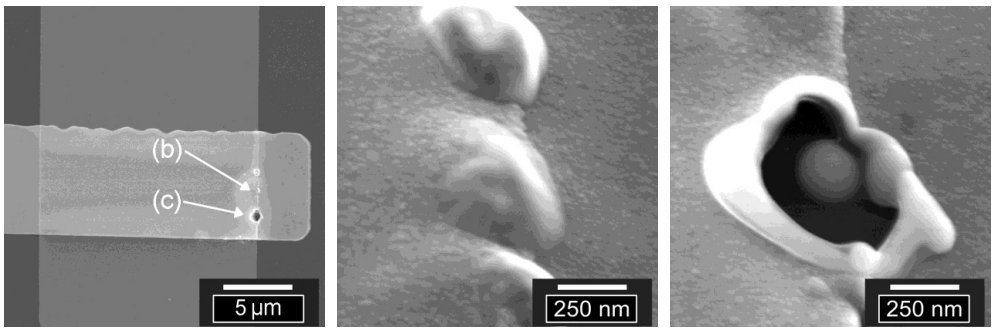
Figure 6.16: (a) *I*(*V*) and *R*(*V*) electroforming characteristic. (b) First set- and reset-sweep after the electroforming. (c) Second switching cycle after electroforming and stable resistance switching with increased ON-current and negative voltage amplitude.

Figure 6.16 describes the adjustment of the electrical parameters. After the electroforming (a) was done, the junction was switched on with a current limit of 100 µA yielding a low LRS of around 2.5 kΩ. This current limit had to be increased to 250 µA during the second cycle to achieve a change of the resistive state (b). Finally, the ON-current and the reset-voltage had to be adjusted within the first 5 to 10 cycles to obtain a stable resistance switching with an appropriate resistance swing (c). The need for a low current limit at the beginning and a subsequent increase of its value suggested a stabilization of the switching mechanism during the first cycles.

Structural considerations

A critical aspect for the integration of resistively switching materials is the change of the morphology during the electroforming. The intrinsic effects, which involved mostly the electroforming but possibly also the subsequent resistance switching, are unknown. Experiments showed strong resistivity degradations during the electroforming process, which are excited by comparatively high currents of several mA in combination with several V, resulting in power densities up to at least several $GW \cdot cm^{-3}$. This value is reduced by nearly one order of magnitude for a quasi-static switching cycle. However, this load is applied several times or rather applied continually during operation.

This fact suggests that the mesoscopic structure of the crosspoint junction might be affected. Several observations, which are rendered in the literature, confirm this conjecture. Szot et al. observed the formation of gas by a bubble under the metallic film of the anode on a $SrTiO_3$ crystal [112]. This effect was also observed in TiO_2 micro junctions, and it is possible that the created gas circumvents the metal film due to its small dimensions or lifts the electrode



(a) (b) (c)

Figure 6.17: SEM images of a crosspoint junction after electroforming. (a) Shown is a large junction with 15 · 7.5 µm². A slight change in the contrast of the image along the edge of the overlap of top electrode and bottom electrode indicated the influences of the electroforming and switching. (b) Detailed view of drop-shaped metal deformations and (c) some burst structures.

partially [57]. A partial destruction of the electrode would not necessarily inhibit the switching effect in a single device. But future structures will use the top electrode of a cell as an input line for adjacent cells, and a complete interruption would isolate neighboring junctions. In combination with TiO_2, an additional impact of the electroforming process on the electrodes was detected [63]. Two different implications on the electrodes were described depending on the direction of the electroforming process. In the case that the top electrode is used as an anode, the metal film is peeled off at the electrode edges. In the inverse case, where the top electrode is used as the cathode, a protrusion in addition to the peeling was observed. Both issues showed a strong impact on the morphology of the electrodes.

The fabricated structures within this study were examined by SEM as shown in figure 6.17, exemplarily. The picture shows a typical crosspoint junction with a 7.5 µm wide top electrode and a 15 µm wide bottom electrode. The central region of the top metal seems to be in its original condition, whereas the edges of the electrode appear brighter. The reason could not be clarified by further SEM examinations, but in comparison with results by Jeong, it appears that structural changes between the TiO_2 and the bottom electrode, respectively within the TiO_2 thin film might be an explanation. The perceptible surface structure of the Pt did not show any changes in comparison with the rest of the metal film. A change of the TiO_2 volume in combination with a distortion might therefore be possible as well as the described creation of cavities due to a gas elimination. The principle geometry of the junction led to an inhomogeneous distribution of the electrical field, which corresponds well with the occurrence of this effect along the edges. Small drop-shaped metal formations could be partially found in the same region. The smooth appearance of the surface might refer to a thermal effect, which can be explained by the very high power density. As the drops seemed to have extended the volume, an additional effect was observed. A simple accumulation of metal could be precluded as the drops occurred much localized and the surrounding area was not influenced. Here, the additional creation of gas that expanded the cavities under the molten metal could be a good explanation, which is supplementary emphasized by burst droplets. The latter was however only an

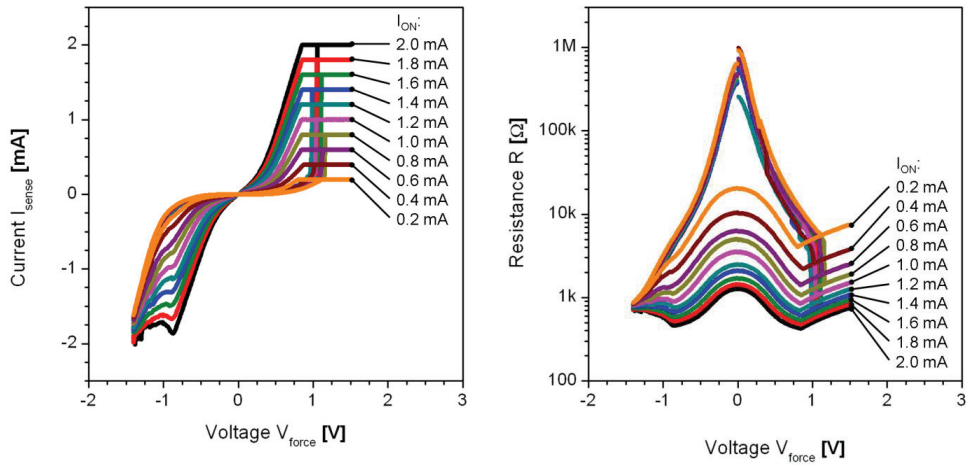
interpretation of the observed effect. It is also possible that the deformation of the electrodes is only the result of heat and not of any participating gases. An indication for the exclusive impact of heat is given by Schmid who describes the consequences of annealing for a combination of Ti and Pt thin films [113].

Finally, the impact of electroforming and resistance switching on the electrode might be critical in regard of crosspoint junctions in the micrometer range. The functionality of single devices was not influenced so far, but the ratio and the absolute area, which was affected by the electrical switching, was much larger than for devices in the nanometer regime, and an interruption of the top electrode would lead to a loss of any junction beyond the broken supply line.

Quasi-static switching operation

As explained in chapter 4, the devices were characterized by two subsequent voltage sweeps, each with a positive and negative amplitude. To obtain a stable switching loop, the ON-current I_{on} of the current limit and the minimum voltage V_{min} had to be adjusted. This was a continuation of the process that is shown in figure 6.16.

Variations of I_{on} and V_{min} resulted in significant changes of the $I(V)$ characteristic. By increasing both values the R_{OFF}/R_{ON} ratio was also increased. Subsequent experiments yielded a reproducible dependency between I_{on} and the LRS as well as V_{min} and the HRS. Figure 6.18 shows the $I(V)$ and $R(V)$ curves of quasi-static measurements with a $10 \cdot 10$ µm² small junction containing an ALD-TiO_2 film. The figure shows qualitatively the dependency between I_{on} and the ON-resistance whereas the minimum voltage for the reset-sweep was fixed to -1.4 V. The device started to switch in a LRS with a current of 0.2 mA. As the programming proceeded in the predefined limit, the exact set-parameters could not be detected. For all subsequent current



(a) (b)

Figure 6.18: (a) $I(V)$ curves with different ON-currents between 0.2 and 2.0 mA for a device with a junction area of 100 µm². (b) Corresponding $R(V, I_{ON})$ characteristics.

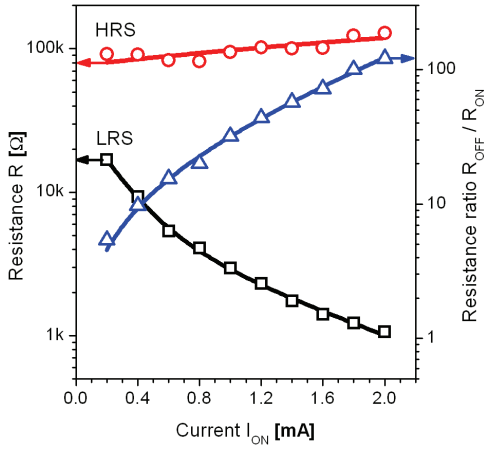
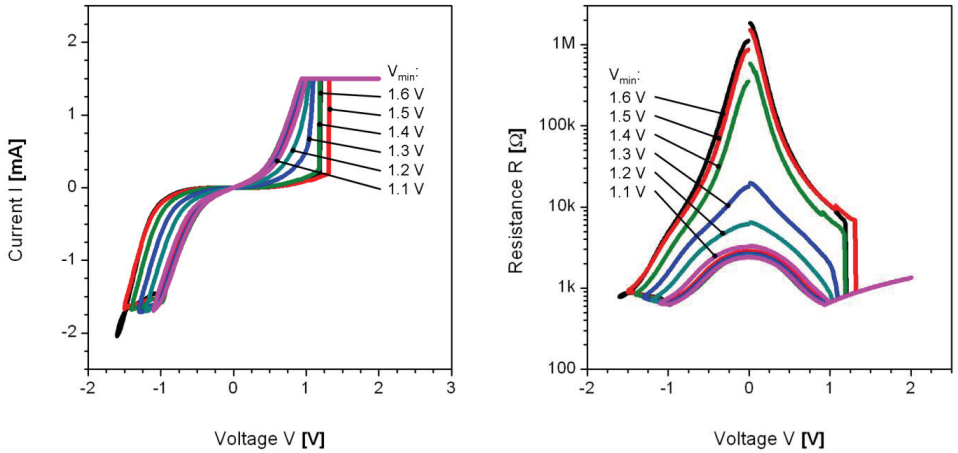


Figure 6.19: Dependency between the ON- and the OFF-resistance and the current limit in reference to figure 6.18. The right axis represents the resistance ratio between HRS and LRS.

limits up to 2 mA, the state changed abruptly around a set-voltage of 1.1 V. As shown in figure 6.18 (a), the curve of the LRS became steeper with increasing ON-current due to a decreasing ON-resistance. The semi-logarithmic scale of figure 6.18 (b) elucidates this dependency. Additionally, the HRS was not affected by the variation of I_{ON}. Figure 6.19 itemizes the exact R_{ON} and R_{OFF} values for an arbitrary read-voltage, V_{READ}, of -0.25 V. The HRS was constantly around 100 kΩ. The LRS decreased nearly exponentially with increasing ON-currents from approximately 20 kΩ down to 1 kΩ. A further increase of the current led finally to a strong degradation of the ON-state and transferred the device in a stable intermediate state. A meaningful value is the resistance ratio between the OFF-resistance and the ON-resistance, which is plotted over the current I_{on}. It increased exponentially, starting below 10 and converging to a value above 100.



(a) (b)

Figure 6.20: Current response of switching cycles with different negative voltage amplitudes modulating the OFF-state of the 100 µm² sized junction.

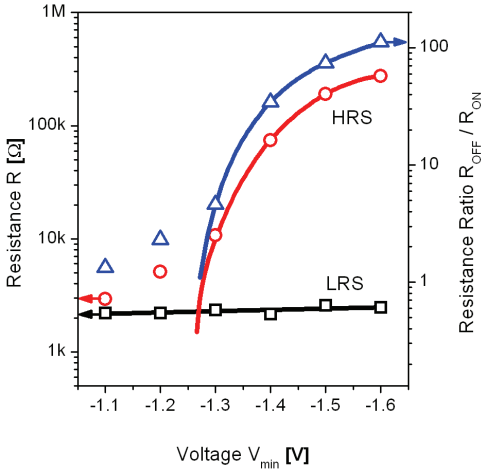
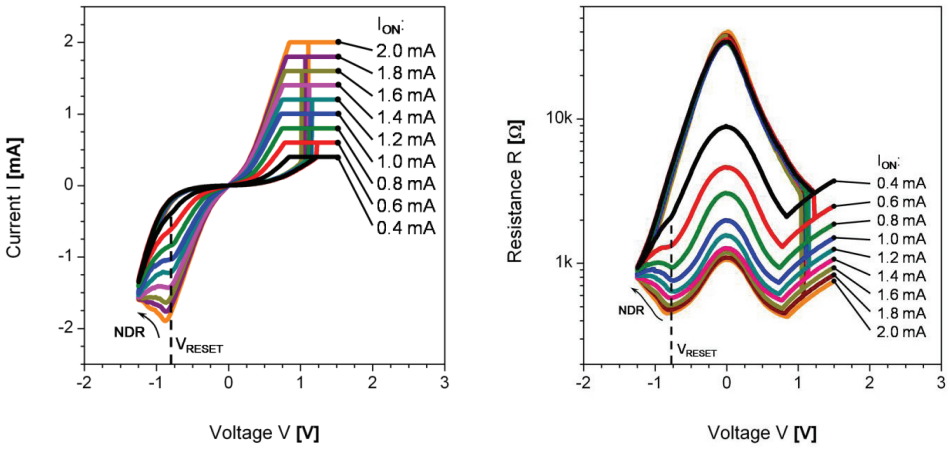


Figure 6.21: Dependency between the ON- and OFF-resistances and the minimum voltage during the reset-procedure V_{min}. The right axis describes the R_{OFF} /R_{ON} ratio.

The HRS could be adjusted by the amplitude of the negative voltage V_{min}. Figure 6.20 (a) shows the extension of the switching loop when the lower boundary of V_{min} was exceeded. For negative voltage amplitudes below 1.1 V, the device remained in its ON-state. However, figure 6.20 (b) shows that the OFF-state increased nonlinearly with voltage amplitudes above this threshold. An initially slight increase resulted in a moderate resistance gain. Then, the resistance rose extremely within the small voltage range between -1.3 V and -1.4 V before it saturated around -1.6 V. A further increase of the negative amplitude transferred the memory cell irreversibly into a degenerated state and led finally to a breakdown. A more quantitative description of the resistances depending on V_{min} at V_{READ} = -0.25 V is given in figure 6.21. The actual HRS gain started around -1.3 V and could be fitted by an exponential function. The LRS was not affected by a variation of V_{min}.

In summary, the operating voltages were adequate with amplitudes below 2 V. However, the occurring currents in the range of 2 mA were only acceptable concerning the device size of 100 µm². The HRS and LRS was controlled by V_{min} and I_{ON} with a nearly exponential dependency resulting in a resistance ratio of more than two orders of magnitude.

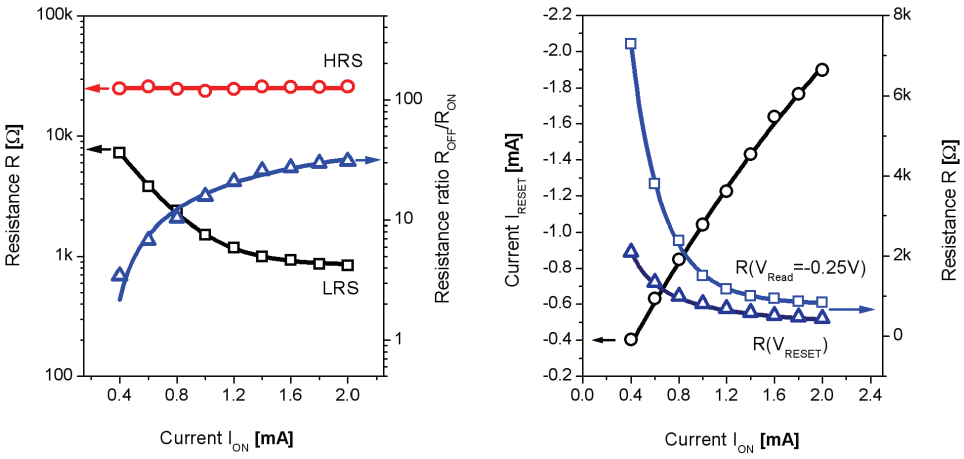
To examine the scaling potential, the junction area was reduced by two orders of magnitude reaching the limit of the optical lithography of around 1 µm. Without changing the material system and the corresponding film thicknesses, the qualitative characteristics of the switching signal were comparable. Figure 6.22 exemplifies the $I(V)$ and $R(V)$ curves of a $1 \cdot 2$ µm² large junction. Here, V_{min} was fixed at -1.25 V and the current limit varied I_{ON} between 0.2 and 2 mA. The device could be programmed with an I_{ON} above 0.4 mA into the LRS, which decreased exponentially with increasing I_{ON} as shown in figure 6.23 (a). This itemizes the exact R_{ON}, R_{OFF} and R_{OFF}/R_{ON} ratio depending on the ON-currents. The HRS was nearly constant whereas the LRS converged exponentially to a resistance of 4 kΩ and the corresponding ratio to a value above 30.



(a) (b)

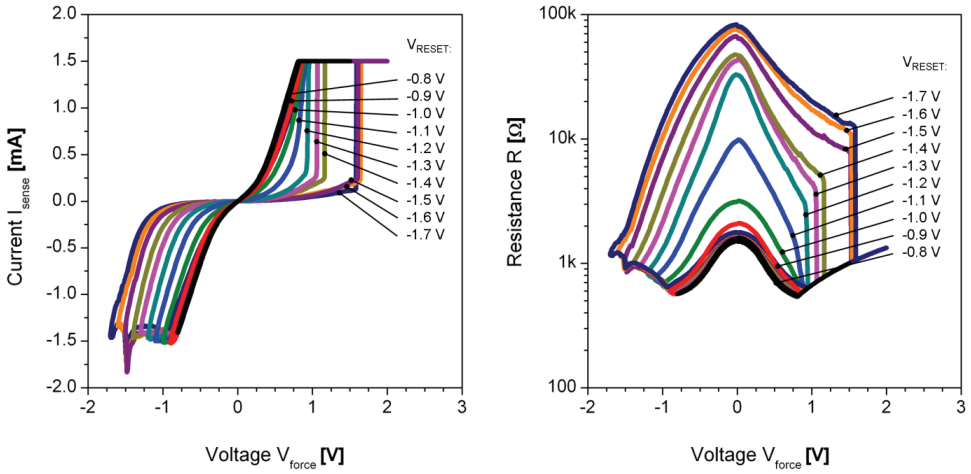
Figure 6.22: (a) $I(V)$ and (b) $R(V)$ characteristics with different current limits I_{ON} for a 2 µm² small crosspoint junction.

The $I(V)$ and $R(V)$ curves in figure 6.22 show also the quasi negative differential resistance (NDR), which involves the reset-process of the device. This is induced by a characteristically sharp bend for low ON-resistances, which blurred however for high ON-resistances. The corresponding reset-voltage was nearly constant with a value around -0.8 V. In comparison with figure 6.18 and 6.20, V_{RESET} is reproducible and independent of the device area and LRS. The reset-current $I(V_{RESET})$ increases nearly linearly with I_{ON} as shown in figure 6.23 (b). The resistance $R(V_{RESET})$ decreases correspondingly ~$1/I_{ON}$, which is in contrast to the R_{Read} and I_{Read} at -0.25 V that could be fitted with an exponential function. The HRS was however constant and independent of the previous LRS, which results in a constant current for V_{min}.



(a) (b)

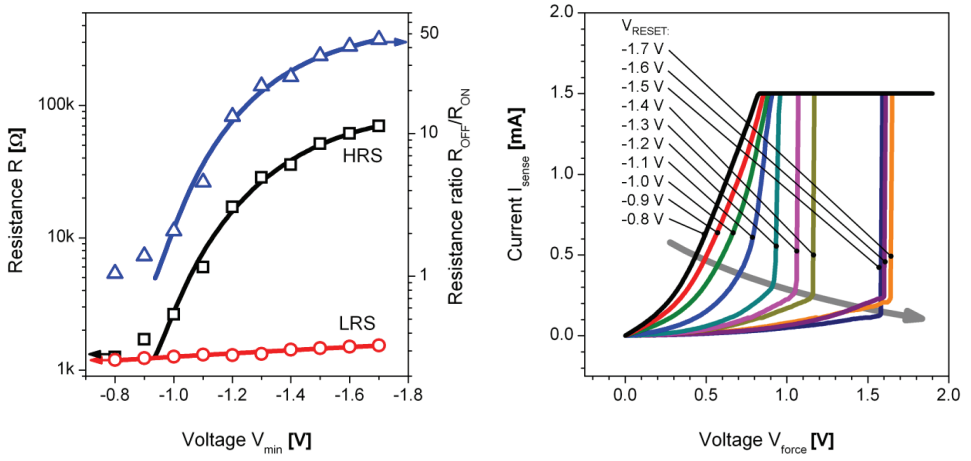
Figure 6.23: (a) Dependency of R_{ON} and R_{OFF} on the ON-current. The blue curve is the resulting R_{OFF} / R_{ON} ratio. (b) Impact of the ON-current on the reset-current in comparison with the relation of the ON-resistance to the reset-current.



(a) (b)

Figure 6.24: (a) $I(V)$ and (b) $R(V)$ characteristics depending on the maximum negative voltage V_{min} for the device corresponding to figure 6.22.

Again, the reset-procedure could be adjusted by the negative voltage amplitude. Figure 6.24 elucidates the increasing HRS by an increasing negative voltage. Without exceeding the reset-voltage between -0.8 and -0.9 V the device remained in its ON-state. At a voltage of -0.9 V, the device started to switch off into the HRS, which increased by a nonlinear function of the applied potential. This property is presented in figure 6.25 (a). Whereas the ON-state was nearly constant, the OFF-state increased moderately for smaller values, but more and more for higher values until the effect seemed to saturate again below -1.7 V. A corresponding R_{OFF} / R_{ON} ratio follows the same characteristic and ends with nearly 50. In spite of this strong influence on the



(a) (b)

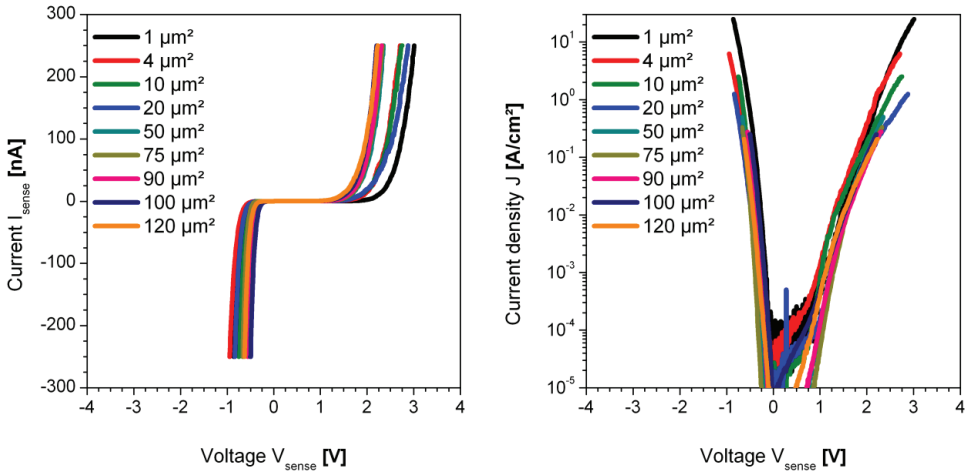
Figure 6.25: (a) Dependencies between the LRS and the HRS and V_{min}. Additionally, the resulting resistance ratio is given (blue). (b) Qualitative description of the set-characteristics depending on the minimal applied voltage during the reset-sweep.

electrical characteristic, the reset-current and voltage were nearly constant and independent of the LRS. This is in accordance with the above given description of the I_{ON} dependencies. As the reset-current changed with the ON-current, the nature of the set- process changed in dependence on the previously applied voltage amplitude. For low V_{min} values the transfer from the HRS to the LRS proceeds in a continuous curve, which is shown in detail in figure 6.25 (b). The course of the switching bends cumulative with increasing V_{min} and results in an abrupt jump for higher HRS. As a tendency, high OFF-resistances caused by high negative voltages led to high set-voltages. A direct quantitative description of any dependency was not conducted due to variations within qualitative results. An example for these variations is the additional peak in the NDR, which resulted in noticeably higher set-voltages of 1.5 V. Several devices with different sizes were tested for a first glance into the scalability of junction areas. However, due to deviations of the current responses that already appeared for different devices with comparable sizes, a quantitative analysis was not achievable. Additionally, the LRS as well as the HRS and the corresponding currents deviated in the range of orders of magnitude. However, due to a constant film thickness, the operating voltages like V_{SET} and V_{RESET} were nearly reproducible. Finally, the reduction of the device size did not constrain the functionality.

In general, the observed characteristics agree with the memristor model, which is described in chapter 2. A negative sweep shifts the positively charged oxygen vacancies away from the TiO_2/Pt interface and increases the Schottky barrier. The switchable element passes into the HRS. In contrast, a positive voltage switches the cell back by shifting the vacancies into the vicinity of the Pt electrode and reduces the barrier width. In the examined case, the frequency of the applied sweeps is very low and nearly constant. However, the spectrum of reachable HRS in the memristor model is continuous and can be modulated by the applied electric field [55]. This can be confirmed by the adjustment of the HRS in dependency of the applied voltage. Additionally, the system seems to be charge controlled, because the LRS can be adjusted by the amount of current that is permitted during the set-process. This could be related to the ionic transport within the bulk, which might be limited by the current or charge (equation 2.13) as well as thermal effects that support the drift of the oxygen vacancies.

6.4 Electrical characteristics of TiO_2 deposited by reactive sputtering

As already mentioned in chapter 3, reactive sputtering is another method to deposit TiO_2 onto a sample. The reason for the implementation of this additional method is given there. In the following section, the electrical characteristics of these thin films are discussed briefly. A comparison between the characteristics of sputtered and ALD-TiO_2 concludes this section.
The dimensions of the used samples for the sputtered TiO_2 are completely comparable with the ones that include the ALD fabricated thin film. The nonlinear initial state of the devices reflects the material, respectively interface asymmetry by a small forward voltage for the negative



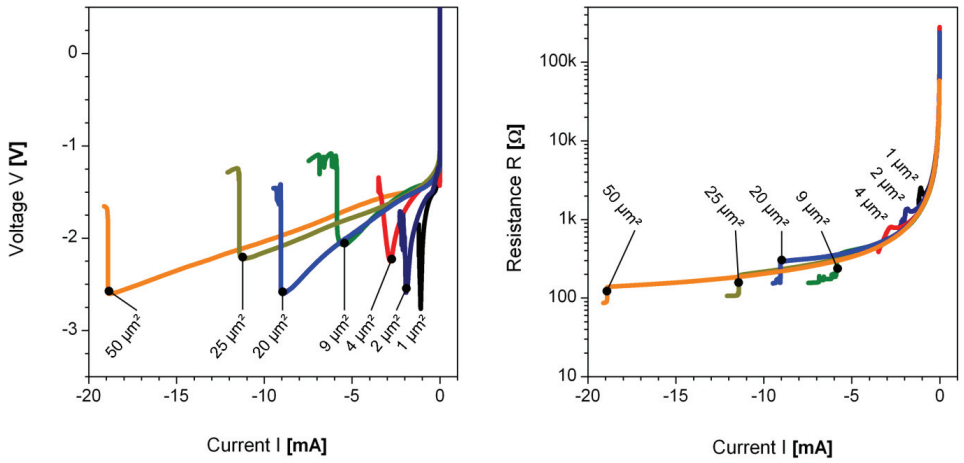
(a) (b)

Figure 6.26: (a) Quasi-static *I*(*V*) characteristic of reactively sputtered TiO_2 for crosspoint junctions with different device sizes. (b) Semi-logarithmic plot of the corresponding current density.

polarity and a higher reverse voltage above 1 V for a positive polarity. In figure 6.26, it becomes evident that the pristine material is not subject to deviations that are as large as those that were found for the ALD thin film. A good agreement within the curves of the current density for different device sizes suggests a nearly homogenous conductance distribution over the junction area. Additionally, the reverse bias of around 1 V is essentially smaller than in the former case (3 V – 4 V).

The exponential characteristic in forward direction, here negative polarity, indicates the existence of a weak barrier between the Pt metal electrode and the n-type semiconducting TiO_2. The opposite interface between the TiO_2 and the Ti can be assumed as nearly ohmic. The higher conductance in forward direction influenced also the forming process.

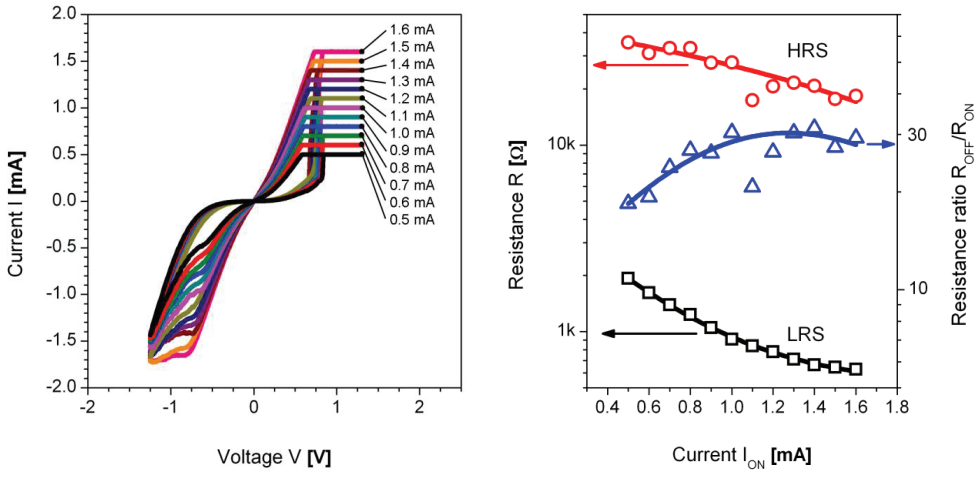
Like for the ALD-TiO_2, a negative current sweep was used to electroform the junctions from the initial state to an OFF-state. The slew rate was again 10 $\mu A \cdot s^{-1}$. Due to the lower resistance, the needed currents were essentially higher than for the ALD layers. As a result, the resistance degradation during the electroforming was very low for large devices. This led to the effect that the forming of areas in the range of around 100 µm² and more could not be observed anymore, because the conductance of the material superimposed the step from the initial state to the OFF-state. Several large devices were stressed by current sweeps up to 30 or 40 mA without a significant electroforming step. However, a resistance measurement after the electroforming showed a significant change. Figure 6.27 shows the dependency of the device size and the electroforming current. This is again increasing for larger devices and is not subject to strong deviations as seen for the ALD-TiO_2. Equivalent to the lower resistance during the forming procedure, the resulting OFF-resistance is also comparably low. As for the ALD-TiO_2, the switching characteristic had to be adjusted subsequently to increase the HRS. This was by trend



(a) (b)

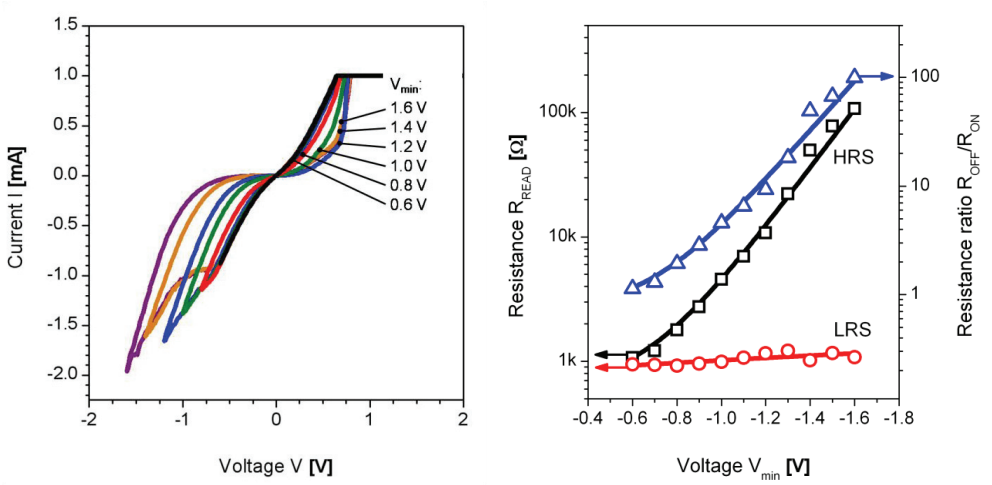
Figure 6.27: (a) $V(I)$ and (b) $R(I)$ characteristics of the electroforming for crosspoint junctions with incorporated sputtered TiO_2. Shown are the devices areas.

very low. In the following the characteristics of a small junction with a size of 1 µm² is compared with the ALD samples. This is done to depict the transferability of the switching characteristics for both deposition methods. However, also the devices with sputtered TiO_2 were subject to strong fluctuations and allow for no examinations related to area sizes. The $I(V)$ characteristic of the 1 µm² large crosspoint is exemplified in figure 6.28 (a). A variation of the ON-current modulated the ON-resistance, which is presented in figure 6.28 (b). For small current limits, the corresponding resistance amounts to several kΩ, but it decreases for an



(a) (b)

Figure 6.28: (a) $I(V)$ characteristic of a 1 µm² small crosspoint junction containing sputtered TiO_2. Shown are the current responses for different current limits I_{ON}. (b) Dependency between the HRS (black) and LRS (red) and the used current limit for I_{ON}. The blue curve indicates the resistance ratio in context of the adjusted ON-state



(a) (b)

Figure 6.29: (a) Modulation of the OFF-resistance by the negative voltage amplitude for the crosspoint junction corresponding to figure 6.28. (b) Interdependence between HRS (black) or LRS (red) and the minimum reset-voltage. The right axis shows the resulting resistance ratios (blue).

increasing current down to several hundred Ω and started to level out for currents larger than 1.5 mA. The approached level could not be measured as the switching became instable for higher currents. Additionally, the OFF-state degraded, although the maximum voltage amplitude for the reset-loop was fixed at -1.25 V. Whether this was a direct response to the modulated LRS or must be addressed to different effect is unknown. From experience, degradation due to high positive currents might be an explanation, as these resulted often in shifts of the HRS and LRS observed for ALD-samples. The result is a saturation and decrease of the resistance ratio beginning at smaller current values. A dependency of the reset-current on the current limit I_{ON} appeared with a comparable increase as shown in figure 6.23 (b).

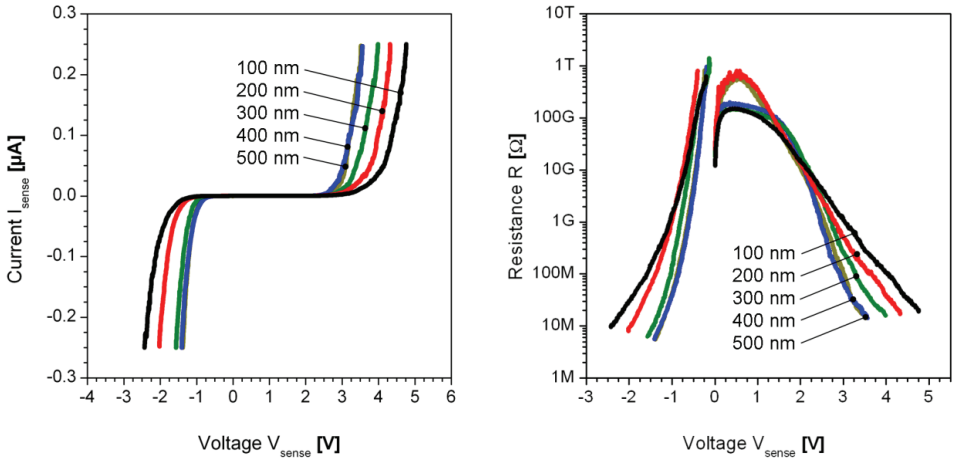
Figure 6.29 (a) presents the $I(V)$ behavior for different V_{min} of the reset-sweep. The influence on the ON-resistance was negligible but the OFF-resistance responded with a large increase of its value over two orders of magnitude. This is also shown by the corresponding resistance ratio in figure 6.29 (b). The influence on the $I(V)$ behavior during the set-process is not shown, but like for the ALD fabricated TiO_2 films the set-loop opens more and more for increasing HRS before the characteristic changed for V_{min} lower than -1.4 V. The reset voltage is in the range between -0.7 V and -0.8 V.

TiO_2 thin films were fabricated by ALD and by reactive sputtering. Both thin films showed resistance switching with an absolutely comparable characteristic. A relation between the characteristics of the ALD fabricated structures with the reactively sputtered structures is absolutely feasible. Same as for the ALD fabricated layer, the reactively sputtered ones yield variations of their characteristics depending on the ON-current during the set- and the minimum voltage during the reset-process. As the presented structure indicated switching parameters in the range of -1.6 V up to 1 V for the control voltage and nearly -2 mA up to 1.6 mA for the current

resulting in resistances between 600 Ω and 100 kΩ, both types are nearly equal. Nevertheless, it is important to mention that the reactively sputtered TiO_2 seemed to be influenced by essentially higher leakage currents. This effect appeared first during the electroforming of larger devices and led to strong restrictions for the values of the HRS. However, a direct relation between leakage currents and device size was not observed. Although the electroforming characteristics of ALD and sputtered TiO_2 differed, the presented electroforming methods could be applied in both cases. After the electroforming, both materials behaved equal, even though their initial properties seemed to be different. Therefore, also an influence on the switching characteristics by the high carbon concentration of the ALD films can be excluded.

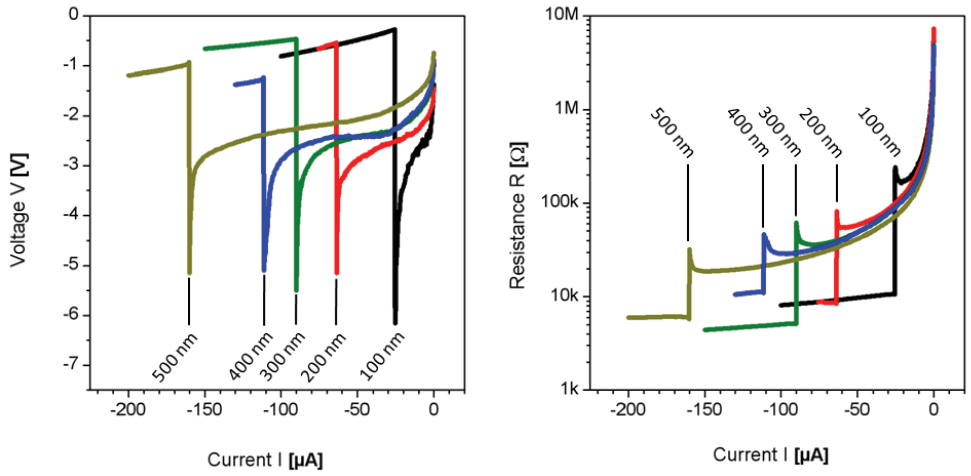
6.5 Switching characteristics in nanometer regime

The current response of a virgin junction directly after the fabrication is demonstrated in figure 6.30. Here, as in the following, a stack of $Pt/TiO_2/Ti/Pt$ is considered with thicknesses of 25/30/5/25 nm. All devices exhibited the behavior of the weak rectifier, which was already found for micro devices. For the forward direction, the resistance decreased for several orders of magnitude between 0 and -1 V. The path resistance is higher than in the micro devices comparing figure 6.30 (a) with figure 6.26 (a). This is pointed out by the lower inclination of the semi-logarithmic curve for higher voltages. However, a direct comparison was not possible as the layer thickness of 30 nm was different. The reverse direction was subject to a cut-off range from 1 V up to 2 V indicating again the weak rectifier. Figures 6.30 (a) and (b) demonstrate a tendency of dependence between the area and the current. Nevertheless, deviations occurred within the devices of one sample and between different samples caused by the inhomogeneity of the three-dimensional junctions. However, the qualitative behavior of the initial state was a good



(a) (b)

Figure 6.30: (a) Initial electrical $I(V)$ characteristics of single nano crosspoint junctions. (b) Corresponding $R(V)$-characteristic. The measurements are a current response to a fast (25mV · s-1) quasi static voltage sweep that stops at a current limit of 250 nA.



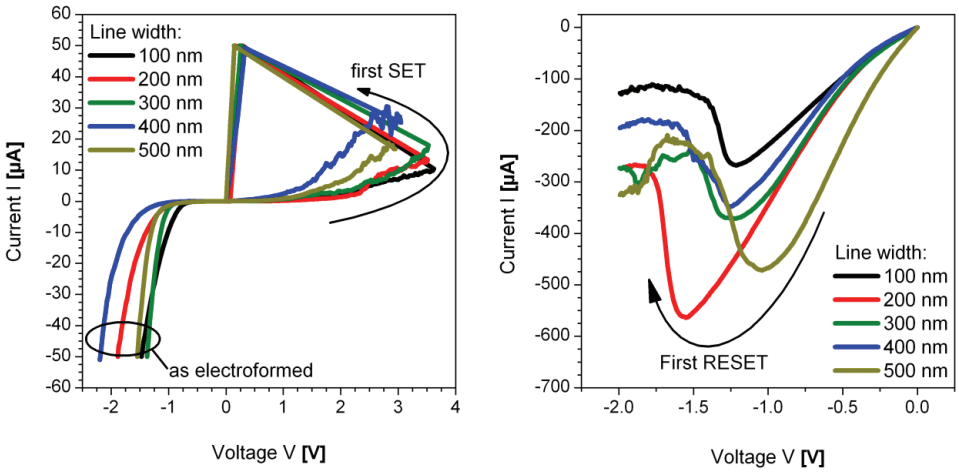
(a) (b)

Figure 6.31: Electroforming process, exemplary shown for nano devices with a junction area between 0.25 µm² and 0.01 µm². (a) The *V*(*I*) characteristics belong to the initial state before the device formed abruptly into the OFF-state. (b) The corresponding *R*(*I*) curves demonstrate a comparable small jump in the forming point.

indicator for a properly working device. Additionally, the downsizing of crosspoint junctions did not influence this characteristic and suggested a simple transfer of the procedural methods from micro to nano devices.

The examination of the electroforming step revealed the advantages of a negative current sweep. This method was also used for the preparation of devices for the subsequent switching analysis. Figure 6.31 (a) and (b) present the *I*(*V*)- and *R*(*V*)-characteristics for all five line widths. The slew rate of 400 nA · s^{-1} was equal for all devices and yielded again a tendency where larger junctions needed a higher current to electroform. This was also in a good agreement with the micro devices. The formed resistance is with 10 MΩ to 100 MΩ essentially higher than the common HRS found by settled switching cycles. As a consequence the set-step needed also a higher voltage to switch the device into the LRS. As indicated in figure 6.32 (a), potentials above 3 V up to 5 V were needed.

The first set-procedure needed a current limit that was essentially lower than the one during the subsequent cycles. Experience showed that 50 µA was normally high enough for a complete transfer into the LRS. Higher current limits often led to a very low LRS that could not be reset. Nevertheless, the obtained ON-resistance was in contrast very low and amounted only to several kΩ. This led to higher reset-voltages and currents, which are shown in the *I*(*V*) characteristic in figure 6.32 (b). At this point the electroforming procedure became random as no dependency between the device size and the occurring parameters could be observed. However, the reset-curve is characterized by a nonlinear shape, where the resistance decreases with increasing voltages. The reset-range itself exhibited a continuous course with a negative differential resistance. Directly after the reset, the current response became noisy while the current settled in the OFF-state. An amplitude of -2 V was sufficient for the first reset into the

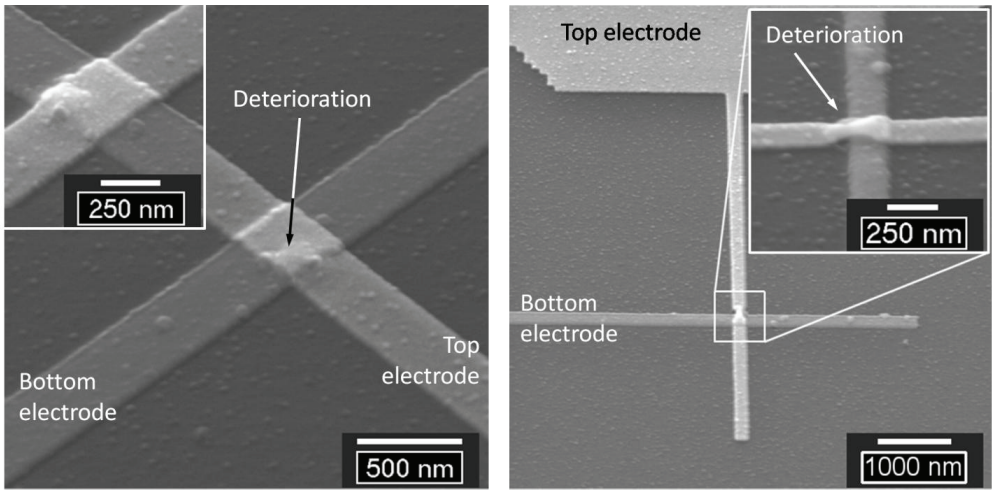


(a) (b)

Figure 6.32: (a) Initial set-process for five device sizes. The I(V) curve for the negative polarity demonstrate the electroformed state. (b) Subsequent first reset-step to switch back into HRS.

HRS. A higher voltage led to a destruction of the device or to an extremely degraded switching effect.

As already mentioned the electroforming created a change in the morphology of the junctions. For micro crosspoints these areas were partially several µm² large and the question arose whether this effect scales with the device size or limits the size of a junction. Figure 6.33 suggests a decrease of the affected area with decreasing device sizes. The top electrode seemed to be lifted slightly after the forming. However, it was not clear if the TiO_2 film expanded due to a phase change, due to heat or if an additional effect occurred. Narrower electrodes, as in



(a) (b)

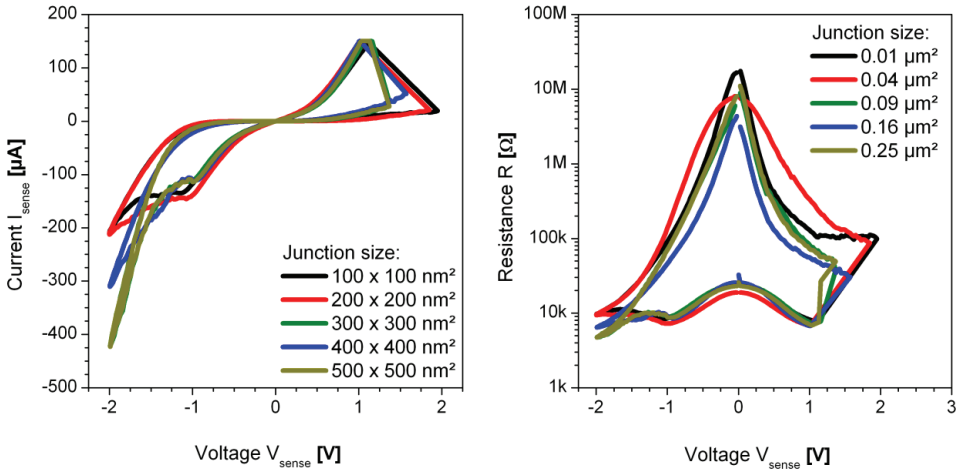
Figure 6.33: Impact of the electroforming step on the morphology of nano crosspoint devices for a (a) 400 nm and a (b) 200 nm wide junction.

figure 6.33 (b), showed a pinch-off of the top electrode along the junction. The surface changes, which could be resolved by the SEM, indicated a thermal contribution as the surface of the metal and the surrounding material became smoother. Additional changes caused by subsequent switching cycles were not observed as long as the energetic impact was not essentially increased. However, this effect did not suppress the functionality of single crosspoint devices down to 100 nm wire width, but has to be considered for further downscaling and application.

Quasi-static switching

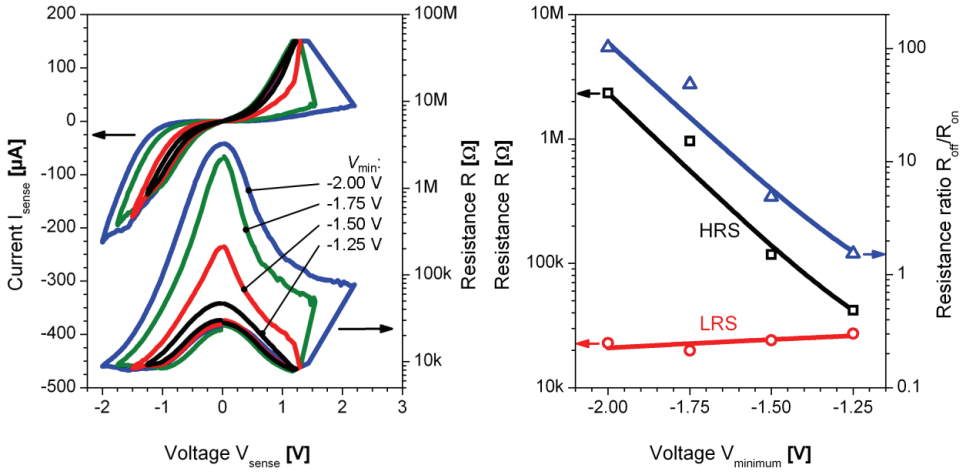
During the switching cycles after the electroforming, the device settled into a stable loop characteristic. This is shown for all device sizes exemplarily in figure 6.34 (a). A scaling of the switching parameters depending on the device size could not be observed. Several devices were tested with a current limit of 150 µA and a reset-amplitude of -2 V. The qualitative nature of the switching was very consistent, but quantitatively the parameters for the HRS state covered a range between 100 kΩ and 10 MΩ. The LRS deviated on the contrary within a smaller range of several kΩ around 10 to 20 kΩ. However, these deviations occurred for 0.25 µm² as well as for 0.01 µm² large devices.

As examined for micro crosspoint devices, the nano junctions were tested in regard of their potential for multilevel storage devices. Figure 6.35 demonstrates this effect for different negative amplitudes during the reset-sweep. Again, the LRS was nearly constant whereas the HRS increased considerably by nearly two orders of magnitude. As a result the resistance ratio increased from 1 to 100. Additionally, the characteristic of the set-step was affected by the maximum negative voltage, too. The set-voltage increased and the transfer became more and more abrupt. The gain of resistance ratio due to an increase of the ON-current by the current



(a) (b)

Figure 6.34: (a) *I*(*V*) characteristic of nano crosspoint junctions with different cell sizes between 0.25 µm² and 0.01 µm². (b) Resulting resistance values were subject to deviations but showed no direct dependency with the incorporated area.

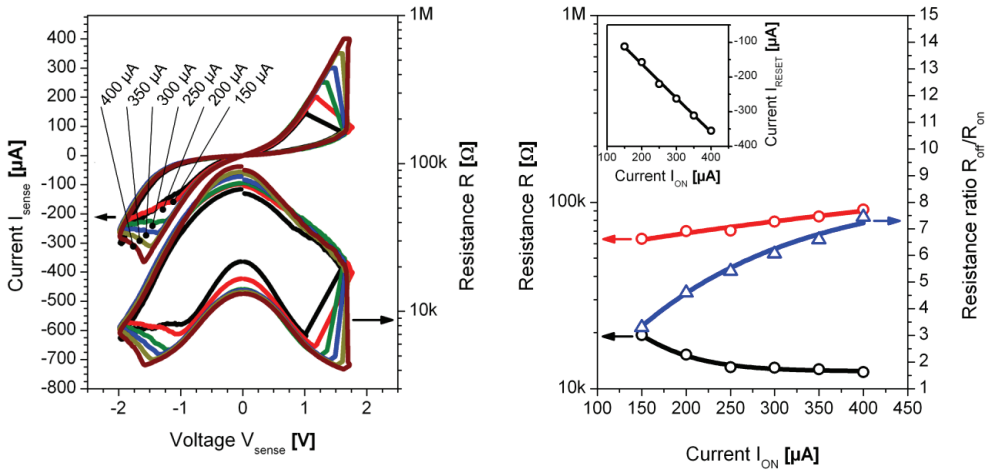


(a) (b)

Figure 6.35: Modulation of the HRS state by the amplitude of the voltage during a quasi-static negative sweep. (a) $I(V)$ and $R(V)$ characteristics showing the development of the abrupt jump and the increase of the set-voltage as well as the increase of the HRS. (b) The LRS is nearly constant whereas the HRS increases clearly (black curve).

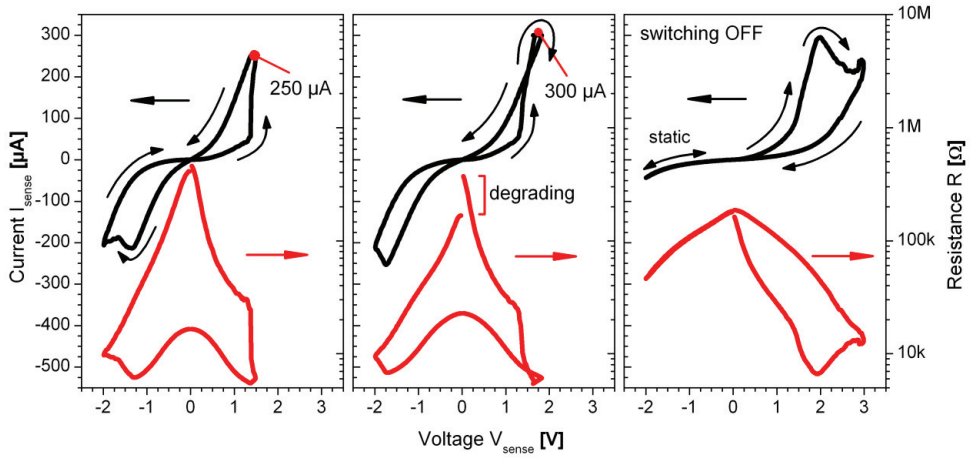
limit was essentially smaller than for the micro devices. For small values a slight increase arose but the LRS stabilized for higher values. The gain shown in figure 6.36 was caused mainly by a shift of the HRS. Nevertheless, the inset in figure 6.36 (b) exhibits the direct dependency between the ON-current and the reset-current, which was also examined in the cases where the ON-state was constant.

A fast degradation of the ON-state was found in several quasi-static measurements with elevated current limits for the set-procedure. The reason becomes obvious by figure 6.37. For a



(a) (b)

Figure 6.36: (a) Modulation of the LRS by the ON-current after the quasi-static set-operation with corresponding $I(V)$ and $R(V)$ characteristics. (b) Illustration of the resistances depending on the current limit. The inset shows the dependency between the ON- current and the reset-current.



(a) (b) (c)

Figure 6.37: (a) Characteristic of resistance switching with a current limit of 250 µA. (b) Degradation of the switching characteristics for an elevated current limit of 300 µA. (c) Inverse reset-switching in the set-cycle.

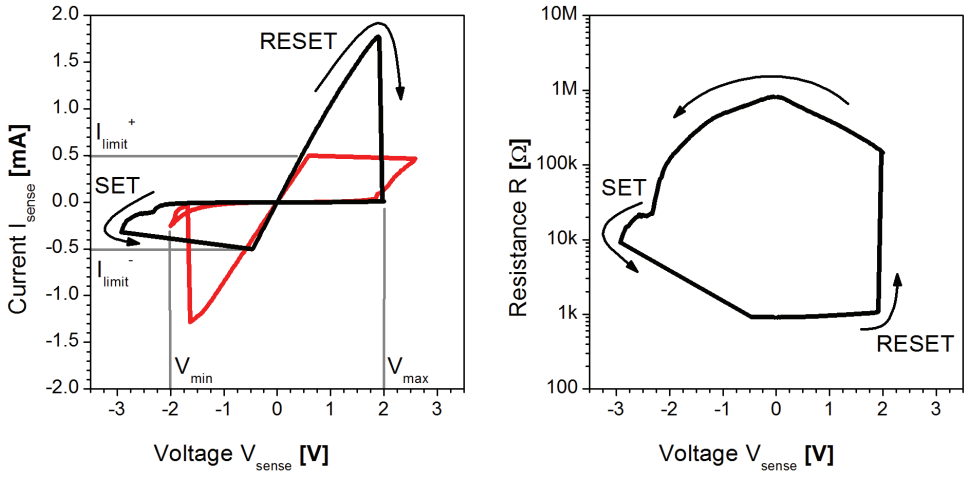
current limit of 250 µA, the switching cycles were stable as shown in (a). The first set-step with a higher current limit, here 300 µA, shifted the ON-state slightly into a higher ON-resistance, illustrated in figure 6.37 (b). This created a second intersection of the $I(V)$ curve during the set-sweep and was the result of resistance degradation in the LRS. Additionally, the HRS was also degraded, which refers to a change of the complete system. An explanation might be a depletion of oxygen vacancies within the conductive channel near the anode (TiO_2/Ti interface). Additionally, it cannot be excluded that the Ti layer oxidizes during the operation resulting in a symmetric system with two Schottky barriers. However, the second positive sweep led finally to a set and a subsequent reset for a positive voltage as shown in (c). The generated state yielded a high resistance and was stable within the tested voltage range. The observed reset-characteristic was comparable to a typical negative reset with an NDR. This suggests the activation of a second switchable barrier with inverted polarities. A further increase of the current limit led finally to an abrupt jump into a very low resistance state with a characteristic that was comparable with the unipolar switching.

As a result, nano devices showed bipolar resistance switching that is absolutely comparable with the one obtained by micro devices. However, the current limit has to be reduced to diminish the degradation of the LRS restricting also the potential of a LRS modulation. The maximum voltage amplitude of the reset-sweep modulates however the HRS exhibiting the potential for multilevel switching.

6.6 Unipolar switching in nano crosspoint junctions

Unipolar switching was described in the introduction besides bipolar switching as an alternative possibility to maintain a reliable, nonvolatile storage for information. Additionally to the advantages of bipolar switching, it needs no negative supply voltage and thereby reduces the complexity of the peripheral circuits. Unipolar switching in binary transition metal oxides has been investigated since several decades. Examples for the used materials are TiO_2, NiO and Nb_2O_5 [47-51, 114, 115]. Jeong et al. described the coexistence of unipolar and bipolar switching for TiO_2, controlled by the initial current limit [111]. Whenever the limit had a high value, unipolar switching occurred, whereas a low current limit led to bipolar switching characteristics. As a result, unipolar switching in TiO_2 was always involved with higher currents in the mA range. Due to a high current limit in voltage driven electroforming steps or a high current limit during the bipolar operation, several devices transformed from the bipolar into the unipolar switching characteristic. The unipolar switching is explained by the fuse / antifuse model that describes the reset-process by a thermal rupture of a metallic element in the material.

The corresponding switching curve is shown in figure 6.38. In the HRS, the resistance was not constant and decreased nearly linear with increasing voltages before it became instable and switched back into the LRS. This switching behavior showed also no negative differential resistance, which is typical for the bipolar switching. As illustrated in figure 6.38, the device could be switched in both polarities and can be described as nonpolar. The switching direction could simply be changed by exchanging the corresponding current limit I_{max} and voltage amplitude V_{max}, shown by the red and black curve in figure 6.38 (a). The associated $R(V)$ characteristic (figure 6.38 (b)) indicates an R_{OFF} / R_{ON} of nearly three orders of magnitude.



(a) (b)

Figure 6.38: Unipolar switching of a 500 · 500 nm² large single crosspoint junction. (a) The $I(V)$ measurement was performed with both switching polarities. (b) Corresponding $R(V)$ curve is shown for one cycle direction.

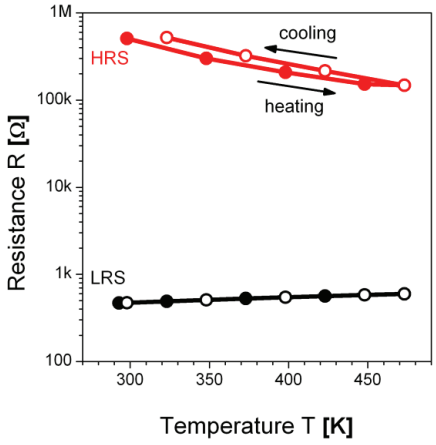


Figure 6.39: Current depending on temperature for the high and low resistance state of unipolar switching.

The resistance was examined in respect of its temperature dependency to assure that this ON-state was different from the ON-state of the bipolar switching. Figure 6.39 shows the resulting resistance at a voltage of 0.5 V for a temperature range between room temperature and 200°C for a heating and a cooling cycle. Whereas the ON-state resistance increased with increasing temperature, which is the typical behavior of a metal phase, the OFF-state resistance decreased. In the typical bipolar switching, the resistance of both states decreases for increasing temperatures. This proved that the examined ON-state was different from the bipolar LRS and belonged to unipolar switching.

Unipolar switching yields a higher ON / OFF ratio, but the applied voltages as well as the currents are essentially higher than for the bipolar switching. These currents were in the end too large for the developed structures and destroyed them.

In the presented example, a current of 1.77 mA is needed to reset a $500 \cdot 500$ nm² small device at around 1.9 V. The measured resistance amounts to 1 kΩ, whereas around 680 Ω are related to the metal electrodes. As the power $P = R \cdot I^2$, most of the power dissipates along the

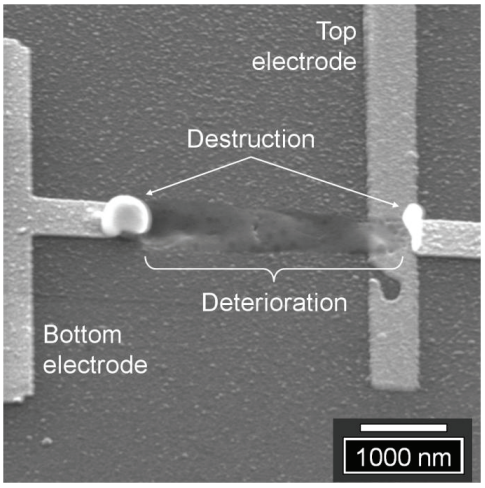


Figure 6.40: Fused 500 nm wide nano wire of a single crosspoint junction. The destruction is the result of high switching currents that emerged by unipolar switching.

supply lines and not in the junction itself. More specifically, the power fraction at the junction is around 1 mW with a voltage of about 610 mV. The remaining power of 2.13 mW drops along the wire. While operating the device, the supply lines suffer under the permanent current flow, which might result in structural changes in the beginning, but led finally to the destruction of the electrode as presented in figure 6.40. From there, it becomes obvious that the unipolar resistance switching in TiO_2, which is described in literature, induces an electrical overcharge. This can be bypassed by a redesign of the electrode assembly, a different controlling setup like short pulses or the reduction of the occurring currents, e.g. by a different material.

7 Considerations of TiO_2 for ReRAM applications

The previous chapters described the properties of nano metallization lines and test structures. To provide evidence of a successful implementation of the crossbar architecture for passive ReRAM, practical investigations have to be performed. The following chapter includes a retention test to prove the nonvolatility of the material system. Also the temperature stability is tested to check the suitability for a future application at operating temperatures. An additional question concerns the switching performance of nano junctions in pulse mode operation in combination with an adjustment of the resistive states. Finally, the application potential of the Pt/TiO_2/Ti/Pt system in a crossbar array is examined with regard to an intrinsic interaction of adjacent cells and crosstalk by the passive architecture.

7.1 Retention in nano crosspoint junctions

To examine the nonvolatile properties, 0.01 µm² small junctions were tested in respect of the retention of the written information. The result is given in figure 7.1. The junction was electroformed by the standard routine and switched for several times to check the functionality. Then a reset was performed and the state was checked after different time periods with voltage sweeps of -0.25 V. This procedure was performed for more than 10^5 s before the device was switched back by a set-step.

An additional check of the functionality demonstrated no effect caused by the retention test, which was also conducted for the LRS, lasting more than 10^5 s. Finally, the device was tested again in regard to its functionality. The retention was verified for more than 10^5 s for both states and showed no degradation. On the contrary, the LRS was very constant whereas the HRS state

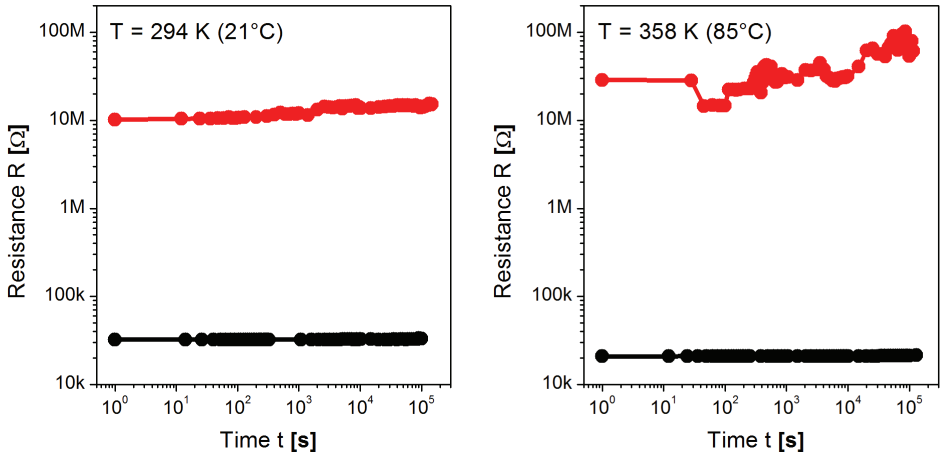
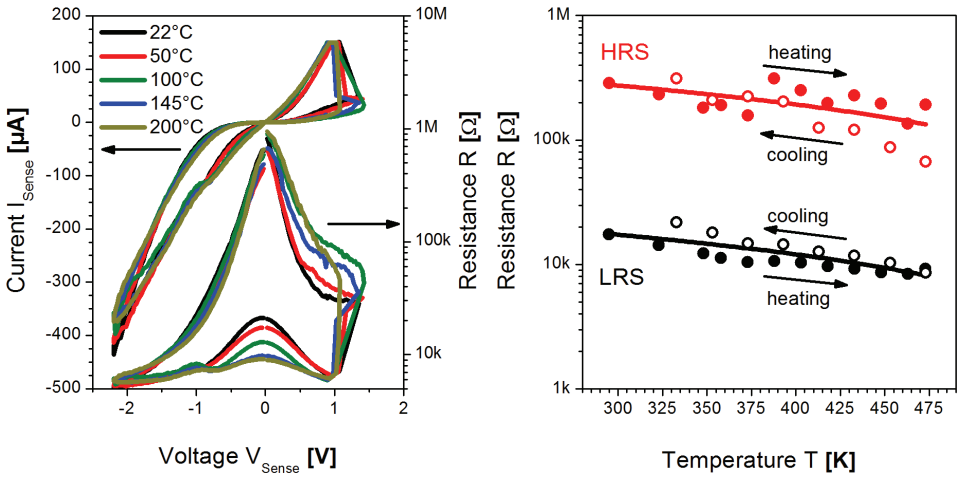


Figure 7.1: Retention measurement for more than 10^5 s at a 0.01 µm² small nano crosspoint junction (a) at room temperature and (b) at elevated temperatures of 85°C.

slightly increased by-and-by, which was a hint for a very stable system in regard of nonvolatility for an even longer period. To check this behavior also for elevated temperatures, the same test was performed at 85°C. Therefore, the device was heated and switched for several times before it was finally reset into the HRS. Then, the periodic read-sweeps were performed, which yielded only small fluctuations, however, the tendency pointed to an increase of the HRS. Subsequently, the junction was switched again for several times and was left in the LRS where it was checked for more than 10^5 s. Also here, the written state was stable and constant as found for room temperature. A final test still showed good switching properties also at higher temperatures.

7.2 Temperature behavior of bipolar switching

Retention tests showed the nonvolatility of the reactively sputtered TiO_2. The test was performed at room temperature and at 85°C, which should simulate a warmed-up system. Due to the heating by a current flow through the metallization lines and the devices, it was feasible that the cell heats up during the operation. By the heat transfer through the metal electrodes and the ambient material also nearby junctions are affected. Thus it is straight forward to switch and to operate a device at higher temperatures. For this reason, a nano crosspoint junction was switched while the complete sample was heated up to 200°C. Figure 7.2 (a) shows the $I(V)$ and $R(V)$ characteristic during the heating, displaying stable switching curves up to 200°C. The HRS and the LRS decreased with increasing temperature, as also described in figure 7.2 (b). This was confirmed by additional tests where each state was written once before the device was heated-up and characterized. These tests yielded short-term temperature stability for the operated material system, which is satisfying as a permanent heating above 100 °C is not expected.



(a) (b)

Figure 7.2: Temperature dependency and stability during quasi-static switching cycles. (a) $I(V)$ and $R(V)$ characteristics between room temperature and 200°C. (b) Dependency of the read-voltage at -0.25 V on the temperature.

7.3 Pulse controlled switching

Quasi-static sweeps are useful to investigate the basic parameters of switching devices by an application of a very slow signal with slew rates in the range of 1 $V \cdot s^{-1}$. However, the junctions are operated by voltage pulses for the write- and read-operation in realistic applications. In addition, pulse measurements are needed to examine the speed of the switching process in TiO_2. These measurements give an insight into the potential of resistively switching systems, related to fast storage applications and market demands. The actual writing speed for volatile memories (DRAM) is less than 10 ns for standalone and 0.2 ns for embedded devices [29]. Flash memory is nonvolatile, but with writing speeds between 10 ms and 1 µs essentially slower than DRAM. The potential of a stack of $Pt/TiO_2/Ti/Pt$ integrated into a nano crosspoint junction was unknown with respect to switching speed and will be discussed in the following section. The used setup and method for this purpose corresponds to the system described in chapter 3.

7.3.1 Resistance switching with 10 ns pulses

A nano crosspoint junction with a size of 100 · 100 nm², was electroformed by a negative current sweep as described in chapter 5. A subsequent quasi-static switching test proved stable LRS and HRS as demonstrated in figure 7.3. The determined resistances at a read-voltage of -0.25 V were 2.6 MΩ for the HRS and 25 kΩ for the LRS, which implied a resistance ratio of about 105. The operational parameters were -2 V for the minimum voltage amplitude and -0.825 V for the reset-voltage. Besides that, the ON-current limit was 100 µA and the set-voltage amounted to 1.5 V.

The set pulse was defined by a rise and fall time of 2 ns. The pulse duration adds up to 10 ns related to 50% of the maximum amplitude as shown in figure 7.4 (a). In preliminary tests, the amplitude was successively increased up to 3 V until a reliable and stable ON-state was achieved. The red curves in figure 7.4 shows the parameters of the pulses that were predefined by the generator. The black curve is the measured signal. This was received with a Kelvin-

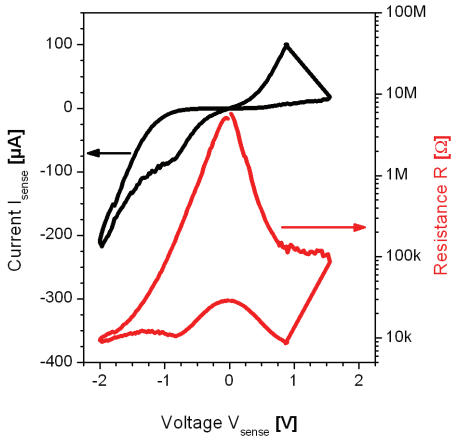
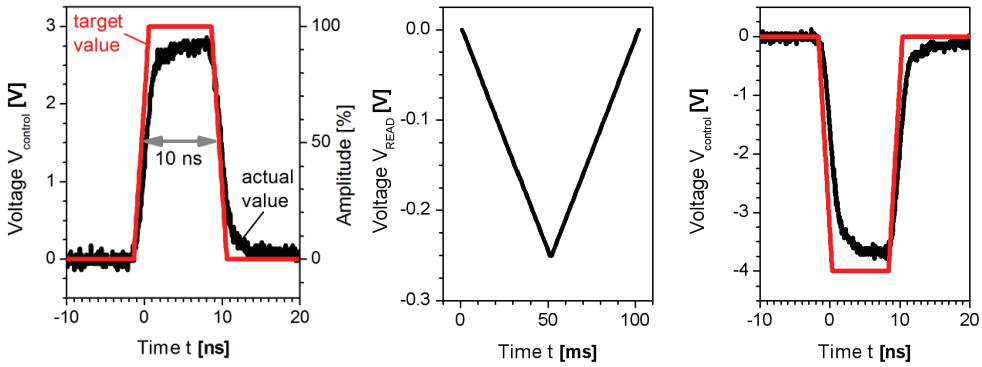


Figure 7.3: Current response of a quasi-static $I(V)$ measurement. The black curve presents the $I(V)$ behavior and the red curve to the concluded $R(V)$ characteristic.



(a) (b) (c)

Figure 7.4: (a) Control signals for the set-, (b) read- and (c) reset-process. The first and the last signal was a 10 ns short pulse, whereas the read-sweep was performed by a quasi-static SMU.

probing setup on the contact pad of the top electrode during the operation (details are given in chapter 3).

The accurate values for the LRS and the HRS were determined with a quasi-static voltage sweep with an amplitude of -0.25 V. This is described in figure 7.4 (b). Finally, a reset-pulse was applied using the same time parameters as for the set-pulse. The amplitude was adjusted to -4 V, where the resulting HRS was comparable with the previously quasi-statically measured value. The reference signal is again given as a red curve in figure 7.4 (c), whereas the black curve shows the actual variation in time.

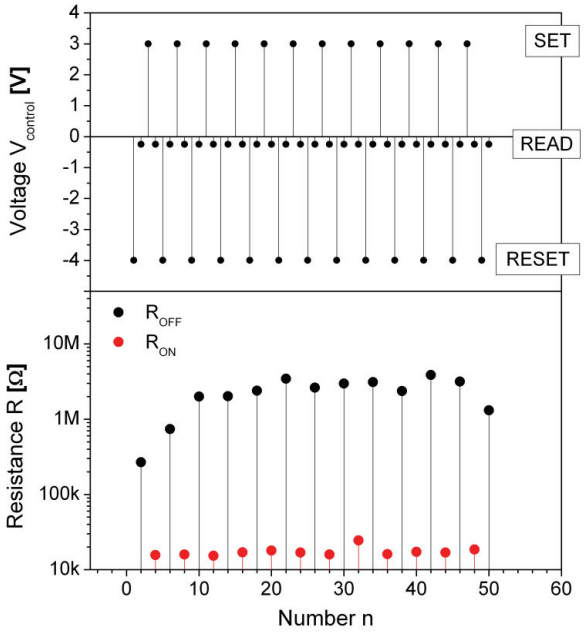


Figure 7.5: Pulse test sequence with 10 ns lasting set- and reset-pulses and interim read-sweeps in the upper part of the picture. The result of the read-sweeps at -0.25 V is given in the lower part of the graph. (HRS (black) and LRS (red)).

Figure 7.5 describes in its upper part the sequence of the control signal depending on the applied voltage. The above described set- and reset-pulses were executed alternately, whereas a read-sweep was performed in between to check the resistive state. Due to the probe tip change, about one minute elapsed before the next step of the routine could be conducted. The OFF-state stabilized during the first pulses and reached a value between 2 MΩ and 3 MΩ. This agreed well with the HRS of the quasi-static characterization. Also the LRS with 10 kΩ to 20 kΩ corresponded to the quasi-static result.

The current and the resulting load during the set- and reset-processes were not limited, which might be a reason for the slight deviation of the resistances. An active current limit with a response time in the range of a nanosecond and without affecting the device characteristic would be a challenge for a CMOS control circuit, which is why this setup met the demands for a realistic device operation in either case.

7.3.2 Pulse amplitude controlled OFF-state variations

Due to the mentioned complexity of a current control for fast pulses in a dynamic system and the low potential for multilevel switching within the ON-state in nano junctions, no examinations in respect of a LRS modulation were performed. The exploratory focus was on the potential of the reset-process that showed excellent multilevel properties, also for 0.01 µm² small devices [116]. In the example, which is shown in the previous chapter in figure 6.35, no current limit was needed and the resistance level was controlled by the voltage amplitude, comparable with junctions in the micrometer range.

In the upper part of figure 7.6, the control sequence for the modulated resistance is explained. The device was switched on with an amplitude of 3 V corresponding to the set-process described in figure 7.4 (a). After the determination of the junction resistance, which was around 20 kΩ, a reset-pulse of -4 V was applied transferring the device into an OFF-state with a resistance of around 4 MΩ. In the following, every reset-pulse succeeded a +3 V set-pulse bringing the device back into the 20 kΩ ON-state. The next reset-pulses had decreasing amplitudes with -3.75 V, -3.5 V and -3 V before the sequence started again with -4 V. The measured resistances were in the range of 1 MΩ, between 300 kΩ and 400 kΩ and finally below 100 kΩ with around 70 kΩ and 90 kΩ. The device showed a stable response over about 200 cycles without any degradation.

This result demonstrated the potential for multilevel switching with fast pulses modulating the OFF-state. No additional current limit was necessary; neither to adjust the state nor to protect the device from overcharging. However, it is important to mention that higher voltage amplitudes beyond 3V or below -4 V and within a pulse duration of 10 ns degraded the switching effect or eventually destroyed the device. In addition, it seemed to be advantageous to perform a set-pulse between two reset-pulses to gain reproducible values even if a transfer from a lower to a higher OFF-state was desired. Otherwise the systems started to drift or became unstable. The explanation is an additional pulse length dependency of the switching effect, which will be

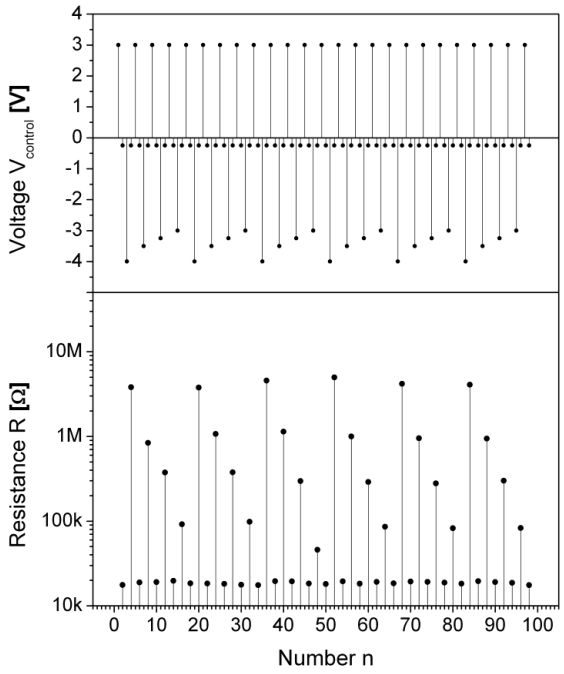


Figure 7.6: Amplitude modulated multilevel switching in a $100 \cdot 100\ nm^2$ small crosspoint junction. The upper half of the figure demonstrates the set- and reset-amplitudes, which induced different reproducible HRS. These are shown in the lower part and determined at a read-voltage of -0.25 V.

demonstrated in detail in the next section. Two subsequent pulses with 10 ns duration and negative polarity correspond to a 20 ns pulse, which generates a completely different HRS. Furthermore, higher voltages of -4 V and +3 V were needed for the operation in the pulse mode than in the quasi-static mode with -2 V and about 1.5 V. This leads to the assumption that the HRS is not simply a field controlled effect. But as the operation time decreased for eight to nine orders of magnitude, the needed voltages just double, which seemed to match with a nonlinear time dependency.

7.3.3 Pulse length dependences of the OFF-state

Due to the conclusion made above, the question aroused whether the value of a HRS could be increased by applying a pulse with a smaller voltage in combination with an increased duration. During the adjustment of the pulses with regard to amplitude and length, transfers from the HRS to the LRS were also observed for smaller amplitudes of 2 V. However, these occurred incidentally. Experiments with several consecutively performed pulses of 2 V and 10 ns yielded no significant result. The extension of the pulse length until the junction switched into the LRS led to a strong degradation of the device due to the lack of a current limit.

On this account, only the adjustment of the HRS with negative pulses was examined. A sequence with five different pulse lengths was applied, as shown in figure 7.7. The primary set-process with +3 V for 10 ns was unchanged, whereas the reset-amplitude was fixed now at -3 V while the duration was successively decreased from 50 ns down to 10 ns. Again, each reset-pulse

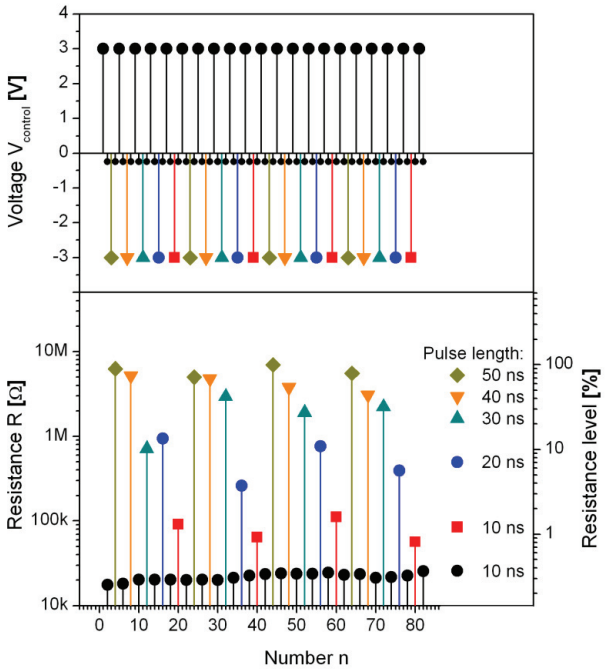


Figure 7.7: HRS depending on the pulse duration of the reset-pulse that is fixed at -3 V. The upper graph describes the switching sequence. Note that each symbol is assigned to a different pulse length. The lower graph shows the result of the read-process. The pulse length is again illustrated by different symbols.

was followed by a set-pulse to bring the device back into the LRS. The right scale indicates the percentage of the OFF-resistance that was reached by quasi-static measurements and a minimum amplitude of –2 V.

The result indicated that an increase of the pulse duration to more than 40 ns created a HRS comparable with the one achieved with an amplitude of -4 V and a duration of 10 ns. Also 10 ns long pulses confirmed the results from former experiments. However, pulse lengths between 10 ns and 40 ns induced huge deviations and less reproducible states. Also in this case, it was recommendable to perform a set-step between different reset-steps, to balance the ON / OFF values and to avoid a drift in the characteristics.

This investigation was completed by the final examination of the time dependency with -2 V reset-amplitudes. The effect was comparable with the one described above for the -3 V amplitude. The results that are presented in figure 7.8 show a lower maximum HRS state than for afore demonstrated devices. The reason was a variation of the HRS for different junctions. Therefore, a reference value was again determined during the quasi-static measurements with -2 V corresponding to 100%. This relative number is depicted on the right scale of figure 7.8. For pulses with 10 ns duration, no reset could be observed. For longer pulses above 100 ns, the device started to switch off with a nearly exponential dependency. It reached the maximum HRS level above 100 µs whereas the OFF-resistance of the initial quasi-static measurement could only be approached approximately. Pulses with an extended duration above 100 µs did not increase the OFF-value, which indicated a slight degradation and confirmed a saturation of the time dependency in this range.

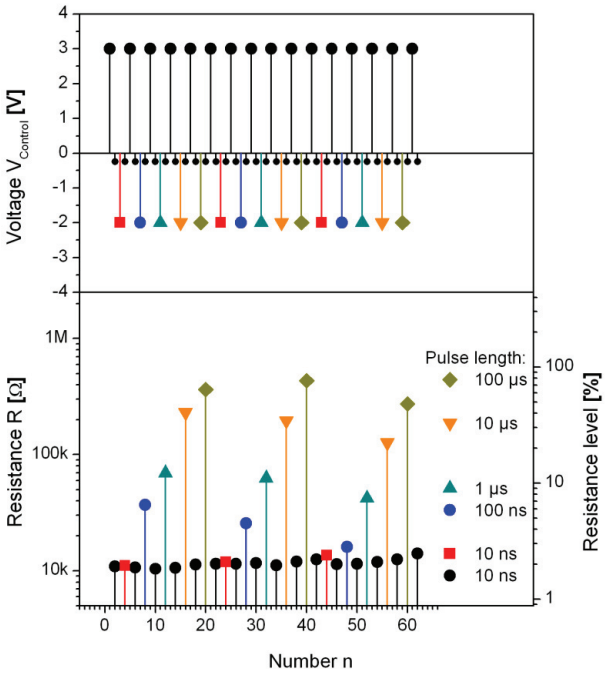


Figure 7.8: HRS depending on the pulse duration of the reset-pulse that is fixed at -2 V.

In summary, it was possible to achieve resistance switching with pulse durations of less than 10 ns, which is compatible with the requirements of future DRAM devices. Comparable results with quasi-static measurements that showed nonvolatility for more than 10^5 s exhibit a device that is essentially faster than today`s floating gate devices. The OFF-state could be modulated between the ON-state and a maximum OFF-value by the amplitude of the reset-pulse. To obtain comparable values with smaller amplitudes of -3 V and -2 V, the pulse duration had to be extended from 10 ns to more than 40 ns and 100 µs, respectively. Pulse lengths between 10 ns and 40 ns or 100 µs created intermediate states, which also offer multilevel switching, although the reproducibility of the time dependant resolution was constricted and led to high deviations. However, the potential for multilevel switching is given by amplitude and pulse length modulation and increases the storage density drastically due to several information bits per memory cell.

Finally, the dependency between the HRS and the pulse length as well as the amplitude is an additional accordance with the memristor model. The oxygen vacancy distribution modulates the resistance state of the element. This is however attributed to the ionic drift that has a corresponding time and amplitude dependency [55].

7.4 Examinations of nano crossbar configurations

The major aim of the following section is the examination of the application potential of passive nano crossbar arrays. Besides parasitic bypasses, which influence the performance of the described arrays, the direct interaction between adjacent junctions needs to be investigated in detail, regardless of the metallic coupling. This means that the switching area of the thin film might be larger than the geometrically defined area of the intersecting electrodes. If one switching path or volume reaches or passes through the adjacent cell, its total resistance is changed and the stored information might be lost. The result would be the loss of addressability of a particular junction and a limit of the scalability.

7.4.1 Operation of a nano word device

These effects can be checked by programming a one dimensional word structure, in which all cells are connected by a common top electrode. The assembly of the electrodes and functional layer is comparable with single junctions. The setup for the electrical test is given in figure 7.9.

The control signal was applied to the top electrode, whereas the bottom electrodes were addressed consecutively by grounding them. All unaddressed junctions were electrically floating. After an initial functionality test of all wires and junctions, the latter were electroformed by the described negative current sweep. Three switching cycles were performed in each case to examine the functionality of the corresponding device. Finally, all junctions were switched off one by one by applying a voltage sweep to -2 V. This reset corresponded to the writing of a logical ‘0’, for example. Then, the complete structure was read junction by junction, using a voltage sweep with an amplitude of -0.25 V. Afterwards, each junction could be addressed and programmed with a logical ‘1’ by a positive voltage sweep with a current limit at 150 µA. Again, the information pattern was checked at -0.25 V. At this point, it was not possible to operate

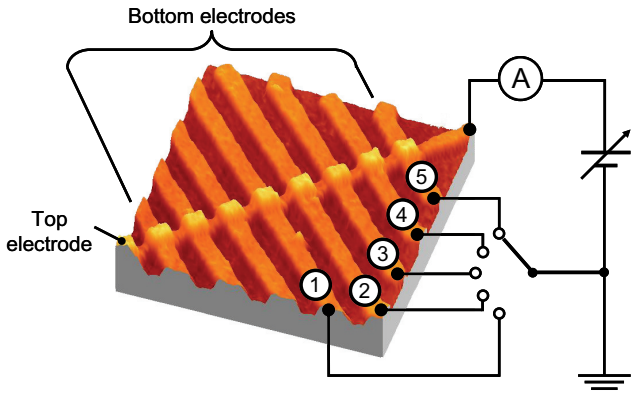
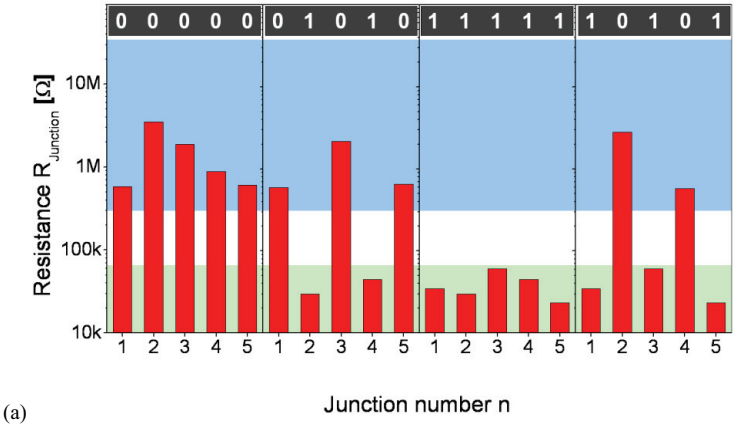


Figure 7.9: Electrical test setup for a nano word device. The top electrode is connected with the voltage source and the amperemeter to record the current response. The addressed bottom electrode is grounded whereas the remaining junctions are floating.

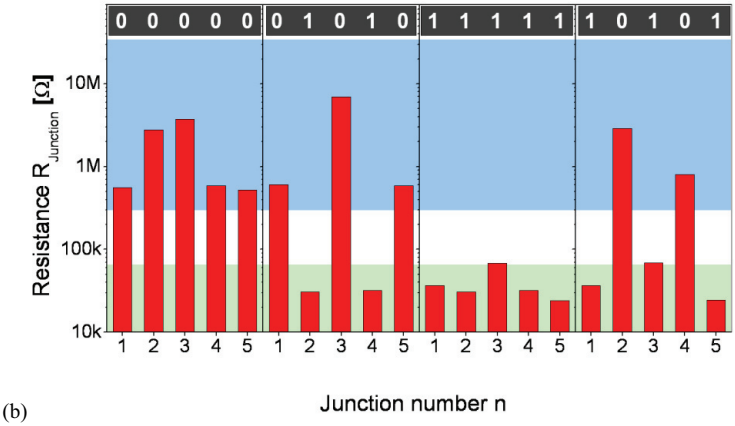
devices with 100 nm half-pitch. As single devices of this size worked properly, it was also possible to operate a single junction within a word. However, the activation of several adjacent junctions was not possible during multiple tests.

Normally, the top electrode sustains an electrical breakdown when two directly adjacent junctions were electroformed or switched, respectively. As the 100 nm electrode was tested with regard to high current loads, a simple overheating was excluded, but the details of the failure mechanism could not be clarified.

On the other hand, devices with 200 nm wide electrodes showed substantially reliable operations. The received resistances of two subsequent tests are illustrated in figure 7.10. Each test contained four information patterns beginning with '00000', which means that all junctions were in the OFF-state. Then, every second junction was switch on leading to the pattern '01010' and afterwards all junctions were transferred into the ON-state, which means '11111'. Finally, every second junction was switched off, resulting in '01010' before the complete sequence started again.



(a)



(b)

Figure 7.10: Test sequence showing the programmed resistances of five adjacent junctions in a word device. Sequence (a) and sequence (b) were performed subsequently. The bar in the upper part of the graph contains the intended state, whereas a '0' represents the HRS and a '1' the LRS.

In general, all considered devices showed a distinct resistance change due to the programming and created a well distinguishable window between the lowest HRS and the highest LRS [116]. The programming of two junctions into a different state did not affect the state of the intermediate junction, which became obvious by the comparison of the resistance before and after the writing process. The sole exception occurred infrequently for the HRS, which showed increased values. But, this was rather a time depending effect progressing into an advantageous direction.

In summary, neighboring junctions, sharing one electrode in a device, do not influence each other, at least not with a distance of 200 nm. The quasi-static switching characteristics are similar to those that were recorded in single junctions. From there, no degradation of the gained resistance values due to crosstalk within the one dimensional device was observed. In conclusion, this experiment showed that the electroforming process is a directed effect between the addressed bottom and the addressed top electrode. First of all, this path is preferred on the basis of the ratio between the layer thickness and the electrode distance within each plane. Secondly, the electric field of the electroforming concerns the switchable volume inside the junction and not between the electrodes of the same level.

7.4.2 Experimental crosstalk considerations in a passive nano crossbar array

The former section showed that no intrinsic parasitic crosstalk occurs for word structures with 200 nm electrode width. This section deals with the crosstalk within an array due to the 2-dimensional crosstalk of metal nano electrodes.

As 200 nm structures showed a more robust behavior, an 8 × 8 bit array with 200 nm half-pitch was examined. The question that is left open cares about the bypasses within a passive array caused by the interaction of cells by the metal lines. Many authors cared in theoretic studies about the addressability of a designated junction in huge and passive networks

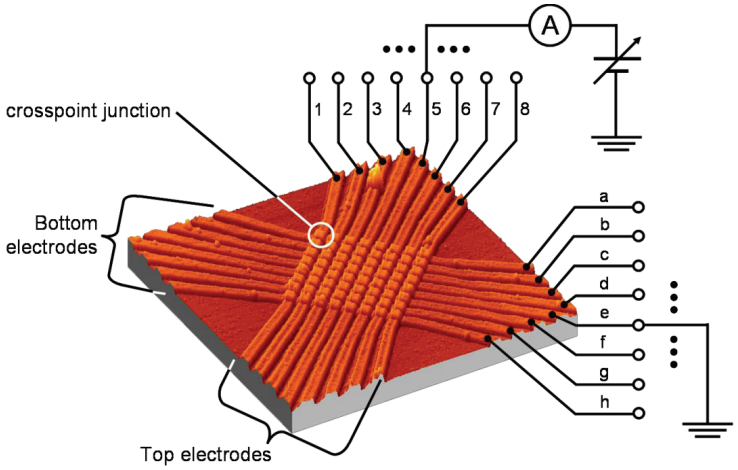


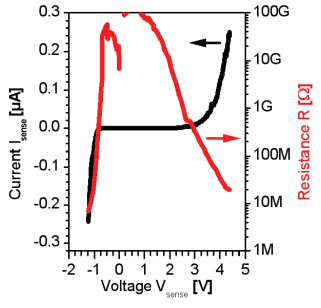
Figure 7.11: Electrical setup for the addressing of an 8 × 8 bit crossbar array with 200 nm electrodes.

[32, 117-122]. This concerns the resistances of supply lines, nano electrodes and junctions in respect of writing and reading operation. Here, this topic was practically examined and will be discussed in the following.

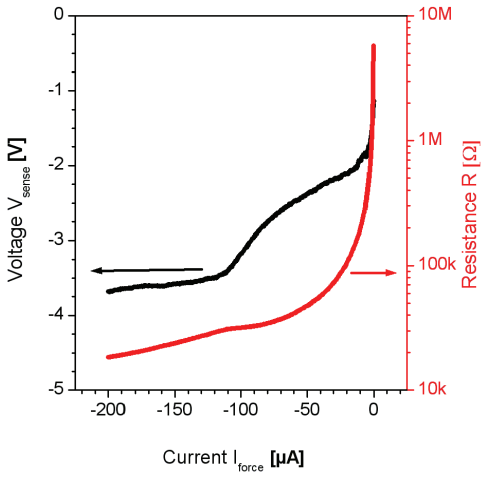
The examination of the above introduced array was performed by the same addressing and operating setup as already described for the word structure. The top electrodes were numerated from '1' to '8' and the bottom electrodes were labeled from 'a' to 'h' as shown in the illustration of the measurement setup in figure 7.11. To address a special cell, the top electrode was connected with the Source-Monitor-Unit, and the corresponding bottom electrode was connected with ground. All other metal lines were floating.

At first, a simple open/short check for each junction was performed by a simple $I(V)$ measurement. Subsequently, the cell was electroformed. Both characteristics are exemplified for one junction in figure 7.12. All tested elements were compared with the behavior of a single and fully functional device showing no significant deviations. However, the voltage response of the forming differed inasmuch as no abrupt branch was observed. After an initially strong decrease of the resistance, the change became smaller. As the current flow was essentially higher than normally needed for junctions of this size, the current sweep was stopped at 200 µA reaching a resistance value of about 20 kΩ.

Afterwards, $I(V)$ characteristics for junction 4d and all eight surrounding junctions were recorded as shown in figure 7.13. The cut-off region in reverse direction vanished completely for the treated device showing the electroforming, whereas all adjacent devices could conserve their rectifying nature. Besides from a reduced resistance in the cut-off region, the electroforming step did not influence the rest of the array, and the addressing of a single device for electroforming was possible. Nevertheless, an explanation for the missing voltage drop in the forming curve might be leakage currents through the complete array structure, which lessen the modification of the corresponding signal. Also this characteristic was observed for all subsequent



(a)



(b)

Figure 7.12: (a) Initial $I(V)$ characteristic of junction 5d. (b) Electroforming course of the corresponding junction.

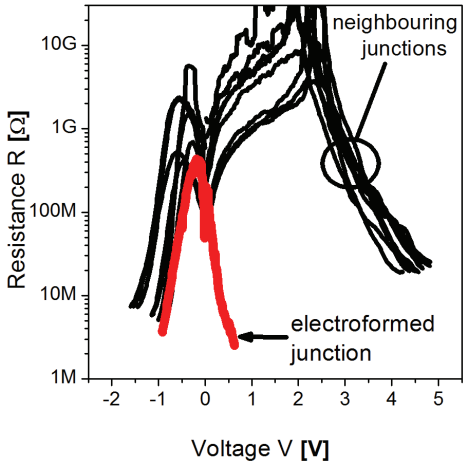
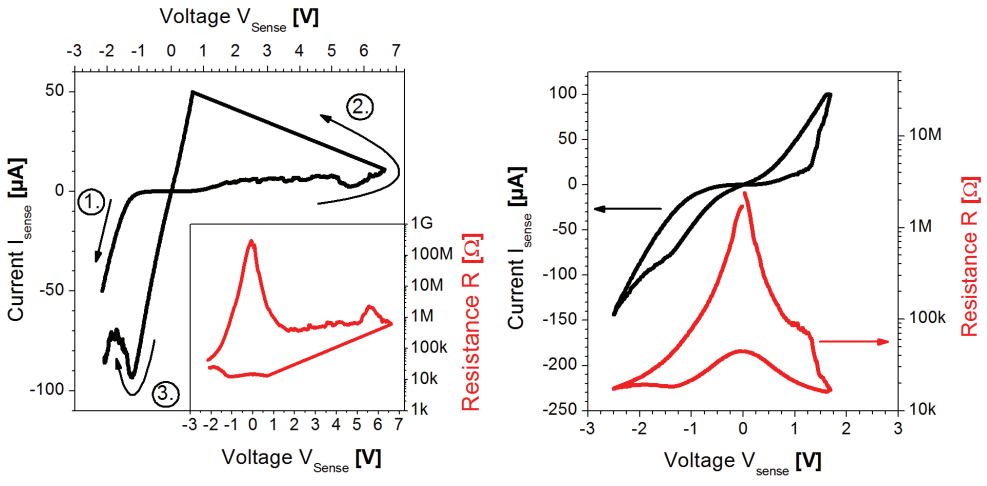


Figure 7.13: $R(V)$ characteristics of the formed junction (red) and all surrounding junctions (black).

electroforming processes within the array. Figure 7.14 illustrates the subsequent switching steps. The resistance that belonged to the first OFF-state was very high resulting in a high set voltage of more than 6.5 V. This might have been an indication that the electroforming step was not fully completed. Nevertheless, the as-formed state and the subsequent switching characteristics were in good agreement with common data. Only the reset-voltage was considerably higher with about -1.3 V compared to the typical -0.8 V to -1.0 V. The explanation is the changed voltage divider caused by the increase of the supply line resistance. Assuming a reset-voltage $V_{RESET}^{(scp)}$ of -0.8 V in a single crosspoint device (scp) and a corresponding reset-resistance $R_{RESET}^{(j)}$ of about 10 kΩ in a junction (j), a voltage divider with a wire resistance $R^{(scp)}$ of 1.3 kΩ is created resulting in the voltage



(a) (b)

Figure 7.14: First voltage cycle (a) of the as electroformed state (1.), the set- (2.) and the reset- (3.) process. The corresponding $R(V)$ curve is given in the inset. Figure (b) illustrates the stabilized $I(V)$ and $R(V)$ curves that belong to the programming of the array.

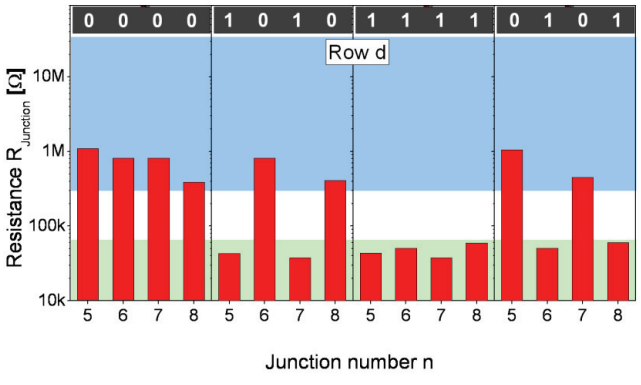
$$V_{RESET}^{(j)} = V_{RESET}^{(scp)} \cdot \frac{R_{RESET}^{(j)}}{R_{RESET}^{(j)} + R^{(scp)}} = 0.71\text{V}\,. \tag{7.1}$$

The resistance of the supply lines in the crossbar array (cba) $R^{(cba)}$ amounts to 7.4 kΩ, whereas the junction dependent parameters are constant. So, the reset voltage $V_{RESET}^{(cba)}$ is

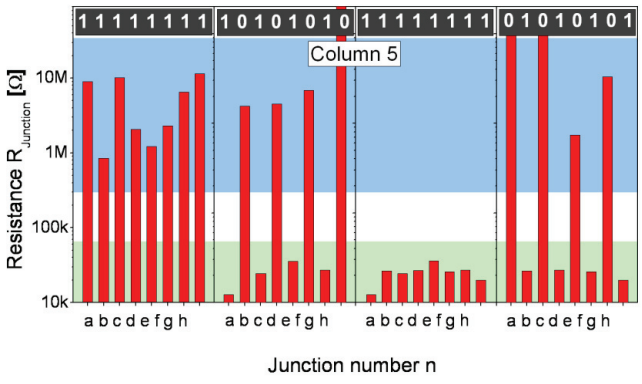
$$V_{RESET}^{(cba)} = V_{RESET}^{(j)} \cdot \frac{R_{RESET}^{(j)} + R^{(cba)}}{R_{RESET}^{(j)}} = 1.23\text{V}\,, \tag{7.2),}$$

which is in good agreement with the observed values. As a consequence of this voltage shift, the reset-amplitude was also shifted from -2 V to -2.5 V.

Finally, the junctions 6d to 8d were electroformed successively and tested. Then, several patterns were written into the half row like already described for the word device. The programmed patterns as well as the resulting resistances are demonstrated in figure 7.15 (a). Like in the nano crossbar word structure, the switching effect of the individual junctions was not affected by the surrounding array. The neighboring junctions were all in the initial high ohmic state. So, any parasitic current was blocked by the high resistances and the fact that always one rectifier was in reverse operation. The latter was however not necessary, which was the result of the electroforming and programming of the complete column 5. All junctions showed a



(a)



(b)

Figure 7.15: (a) Programming sequence of junction 5 to 8 in row d and (b) of the complete column 5.

comparable behavior that was related to the electroforming process and switching characteristics of each cell. Again, these junctions were programmed and read successively as demonstrated in figure 7.15 (b), and no deterioration of the functionality could be observed. Like in the nano crossbar word structure, the switching effect of the individual junctions did not suffer under the existence of the surrounding array.

Finally, the junctions of column 5 and row d could be addressed and operated randomly. The other, unformed crosspoints showed no relevant influence. This was expected as the common operation voltages were between -2.5 V and +2 V. The junction in the bypass was arranged into the opposite direction and therefore operated with voltages between -2 V and +2.5 V. Both voltages are not sufficient for an electroforming step.

This led to the final examination of the electroforming of a junction that built a direct bypass to previously considered cells. Row d and column 5 were aligned orthogonally against each other; therefore any bypass was blocked by an unformed junction. If any other element outside

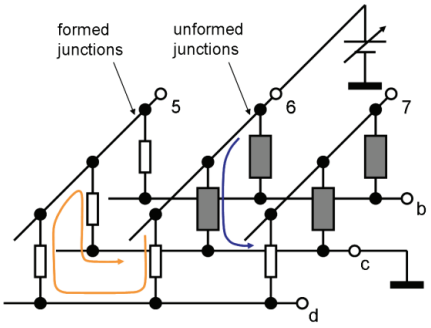


Figure 7.16: Illustration of the bypass (orange arrow) in parallel to the voltage drop along the addressed junction (blue arrow). The white resistor symbol demonstrates switching junctions whereas the grey symbol depicts unformed junctions.

of this pattern was activated, for example 6c, the already electroformed junctions offered a more conductive path for the current. Due to this, it was not possible to record the initial state of this junction. The $I(V)$-measurement of all cells right of column 5 exhibited a nearly symmetrical nature, which was comparable with the ON-state of a junction. Assuming that the addressed cell was still in the initial state, the current response was created by the junctions in the bypass, which is shown in figure 7.16. Current sweeps as well as voltage sweeps were performed to electroform the cell. However, this approach resulted in a combination of set- and reset-processes in the bypass and finally in the destruction or degradation of the participating devices. That 5c, 5d and 6d were involved is shown in figure 7.17. After the electrical stressing of crosspoint number 6c, the junctions 5c and 6d were short circuited, showing a constant resistance of about 8 kΩ. This complied with the resistance of the supply lines. However, junction 5d still had the characteristic of the LRS, but could not be reset, whereas 6c showed nearly the same nature if addressed. At this point it was not possible to assign the original characteristic of one of these two junctions (cell number 5d and 6c), which might have resulted in a combination of both.

The reason is the high electroforming voltage that is needed as shown in figure 6.31, for example. If this voltage is applied to the addressed junction, the three elements in the nearest bypass build a voltage divider with the same voltage drop. Assuming that all devices are in the

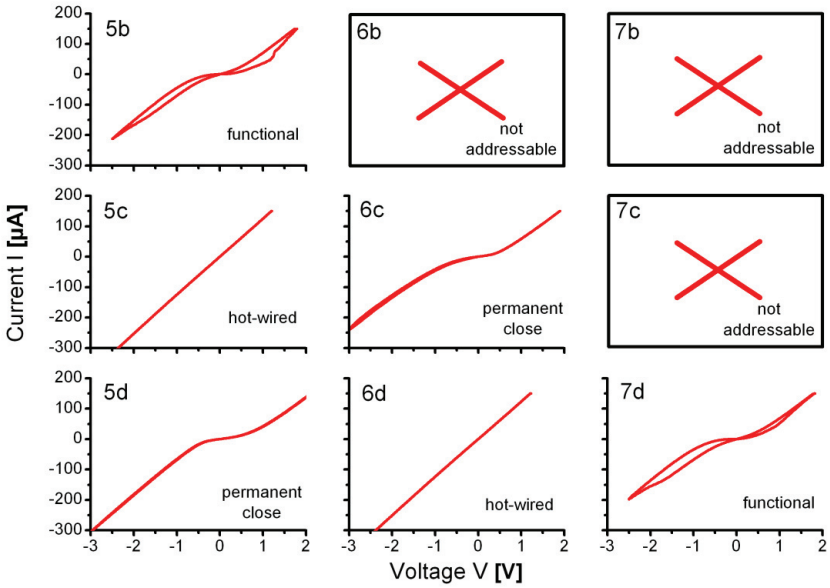


Figure 7.17: $I(V)$ characteristics of the affected junctions after the electroforming attempt for junction 6c. The crossed fields belong to unformed junctions, which were not operated during the examination.

HRS, one element is always connected in set-direction and switches into the LRS once its threshold is exceeded. Due to the missing current limit this will break down, typically into a very low resistance. As a result the voltage drop over the remaining elements increases and exceeds also the allowed value. These junctions degrade or break down, too. This effect is of course depending on the deviations of the participating elements, whereas some show higher thresholds, which might protect the bypass, some might also yield lower thresholds.

The application of voltage schemes, as described in chapter 2, might be a solution if the required electroforming voltage is less than three times larger than the operating voltages V_{set} and V_{min}. Then, the voltage drop over each elements of the bypass can be forced to be one third of the electroforming voltage.

Finally, junction 5b and 7e as well as the rest of the array were still switching and showed no additional degradation. A reversibly programmable array was therefore not achievable. Reducing the functionality to a ROM (read only memory) or a one-time programmable router, the application of an array is an opportunity as described in [21].

The concluding statement for the operation of nano crossbar arrays with 30 nm TiO_2 is that intrinsic interactions between neighboring cells were not observed for electrode distances above 200 nm. As long as always one functional element in any bypass is not electroformed, no parasitic influences in form of current bypasses were observed, at least not to an extend that minimizes the functionality of particular cells or the complete array.

The effect of parallel paths on the switching properties of an array could not be examined, as the prior electroforming tuned out to be a serious issue.

8 Conclusion and Outlook

This chapter summarizes the results of the integration of resistively switching materials into passive nano crossbar arrays. The employed functional thin film was TiO_2 and the metallization lines were a combination of Ti and Pt. This study focused on the fabrication of crosspoint junctions as single memory elements, which were in the first place downscaled into the nanometer range and secondly extended to crossbar arrays. A further aim was the examination of the functionality and the electrical characteristics of the integrated TiO_2 as well as the developed crossbar arrays. The outcome of this study in the extensive field of nano crossbar array applications and resistance switching could be the basis for future intentions and examinations that are addressed in the outlook.

Fabrication and properties of crosspoint and crossbar electrodes

Metal lines with sizes between 15 µm and 50 nm were patterned by lift-off metallization. Optical lithography was used for feature sizes above 1 µm and an electron beam direct writing process was developed for smaller line widths. The Ti/Pt electrodes were deposited by thermal evaporation, but due to the flexible lift-off process a wide range of materials can be applied without any process adjustments. The prototyping by electron beam lithography offered an additional degree of flexibility because a fast revaluation of the pattern was provided without any changes of the process parameters. Due to the high alignment accuracy and independency on the surface roughness, the top electrode fabrication corresponded to the one of the bottom electrodes.

Beneath single crosspoint junctions, several different devices were designed including $1 \times n$ word structures (one top electrode crossing n bottom electrodes) and $n \times n$ arrays with sizes up to $n = 64$ and metal line widths down to 100 nm.

With this method additional test devices were fabricated to examine the resistivity of nano size metal lines. Measurements for Pt conductors yielded a nonlinear increase depending on the dimensions of the electrode cross-section. This was downscaled to about $50 \cdot 30\ nm^2$, which was in the range of the electron mean free path. The received values agreed well with a combined model from Fuchs-Sondheimer and Mayadas-Shatzkes considering the scattering of electrons at surfaces and interfaces. The resistivity of a 100 nm wide Pt line was determined at $37.8 \cdot 10^{-6}\ \Omega\cdot cm$, resulting in a resistance of 25 Ω for the electrode fraction per junction. Compared with the LRS of the incorporated TiO_2, the occurring voltage divider over the electrodes was insignificant for the examined arrays and offered a high potential for further downscaling as well as for an increase of the array size.

The fabricated bottom and top electrodes showed a high yield of robust metal lines. Long-term tests with a load of 1 mA for more than 12 h resulted in no failures for Pt wires with a cross section of $100 \cdot 30\ nm^2$. In conclusion, the generated structures provided a flexible and powerful template for the examination of the scaling potential of different functional materials, and their integration into passive crossbar arrays.

Switching properties of TiO_2 in crosspoint and crossbar arrays

Thin TiO_2 films were applied by ALD and reactive sputtering. Both methods showed good covering properties and a dense layer without any short circuit in a junction. The pristine films were different as ALD created nearly amorphous layers with a high carbon concentration whereas reactive sputtering yielded a phase mixture of anatase and rutile. However, in combination with a Pt and a Ti interface both layers showed initially an asymmetric electrical characteristic with a high resistance.

An electroforming process had to be performed to transfer the devices into a switchable state. This was examined in regard to its polarity and the differences of a voltage or current controlled signal. A negative current sweep offered reliable results, which covered occurring deviations and electroformed the junction into the HRS. Additionally, no current limit was needed to protect the device from an electrical breakdown.

Both fabrication routes yielded a reliable and comparable bipolar resistance switching for junction sizes between 100 µm² and 0.01µm². With operating voltages between 1.5 and 2 V and currents in the range of several hundred µA for devices smaller 1 μm^2 up to 2 mA for larger devices, resistance ratios up to more than two orders of magnitude were achieved. However, a direct quantitative scaling of the current with the device size was not observed. The programming into the LRS was controlled by a current limit and the erasing into the HRS state by the amplitude of the voltage sweep. According to the memristor model, the LRS could be adjusted quasi-statically by the permitted set-current, whereas the HRS could be modulated by the maximum amplitude of the reset-sweep.

By pulse operation, the junctions yielded a switching speed of less than 10 ns and w/e-voltages of 3 V and -4 V, showing the high performance of this material system. In contrast to quasi-static measurements, no current limit was needed during the set-process. Additionally, the HRS could be modulated reversibly in the range between 10 kΩ and several MΩ by the reset-process via the pulse amplitude and pulse length. This extends the potential for multilevel switching by fast pulse operation and increases probably the storage density enormously without any technological expense.

The retention of both resistance states was checked for more than 10^5 s showing no degradation also for elevated temperatures. From this point of view, the device can be regarded as quasi-nonvolatile and also functional at higher temperatures.

The examination of resistance switching in crossbar structures like words and arrays yielded an insight into the static crosstalk or interference between neighboring junctions. Tests showed no switching between the electrodes of one layer below or on top of a TiO_2. Investigations of complete word structures down to a feature size of 200 nm (corresponding to line width and distance) yielded a reliable programming and erasing of different information patterns in adjacent junctions without any resistance degradation. As a result, no intrinsic crosstalk through the TiO_2 was found and no interaction between neighboring electrodes appeared.

Within an array it was possible to electroform and to operate a complete row and column at the same time. The unformed junctions remained in their initial state and the programmed junctions behaved comparable to single junctions. The remaining unformed junctions suppressed parasitic bypasses by their high initial resistance. However, a virgin cell that is parallel to a path of electroformed junctions could not be electroformed while all other lines were floating. The occurring current stressed the already formed cells in the bypass, which were degraded into a permanent closed state.

From there, the pattern of switchable junctions in an array with the examined material system is limited by the electroforming. However, single resistively switching junctions of TiO_2 showed competing and promising properties for the integration into CMOS and, particularly in combination with a select transistor, a future application in a ReRAM device.

Outlook

The fabrication process and the developed crossbar structures provide a general and reliable template in the sub-micrometer range for a multitude of different electrode materials and electrically functional thin films. Considering the electroforming process for TiO_2 with its high voltage and current, it might be possible to decrease these values by adjusting material parameters like the oxygen/ vacancy concentration during the layer deposition or their diffusion paths by the crystal structure. The exchange of the interface materials could additionally influence the switching signal and the endurance by increasing/ decreasing the asymmetry of barriers or affecting the oxidation/ reduction of the involved materials. In this context, the supplemental integration of a diode-like, nonlinear element by an appropriate material combination could increase the performance of a passive array with respect to the suppression of parallel parasitic paths.

Apart from epitaxial material systems, this experimental platform can also be used to examine completely different material systems in regard to their switching scalability and suitability for passive memory arrays and logic. Within this study with TiO_2 the focus was on 100 nm small feature sizes. However, this lift-off technique provides room for optimization and allows a further downscaling of the metal line size into the range of several ten nano meters for the examination of scalability limits.

Small MIM structures containing TiO_2 showed good results for integration in combination with a transistor in a 1R1T memory device or as a limited pattern of reconfigurable switches for routing and logic applications. Therefore, the presented fabrication process in combination with the used material system is feasible for a setup of a hybrid system, containing CMOS architecture and resistively switching TiO_2 cells. This could be used as a general technology sandbox for the evaluation of hybrids concerning the fabrication process, particularly the interconnection between both layers and the operation of resistively switching materials by common CMOS architecture. With a corresponding modification of the electrical characteristics, the complete passive array could be used as a core component to test passive ReRAM and logic applications in a hybrid structure.

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